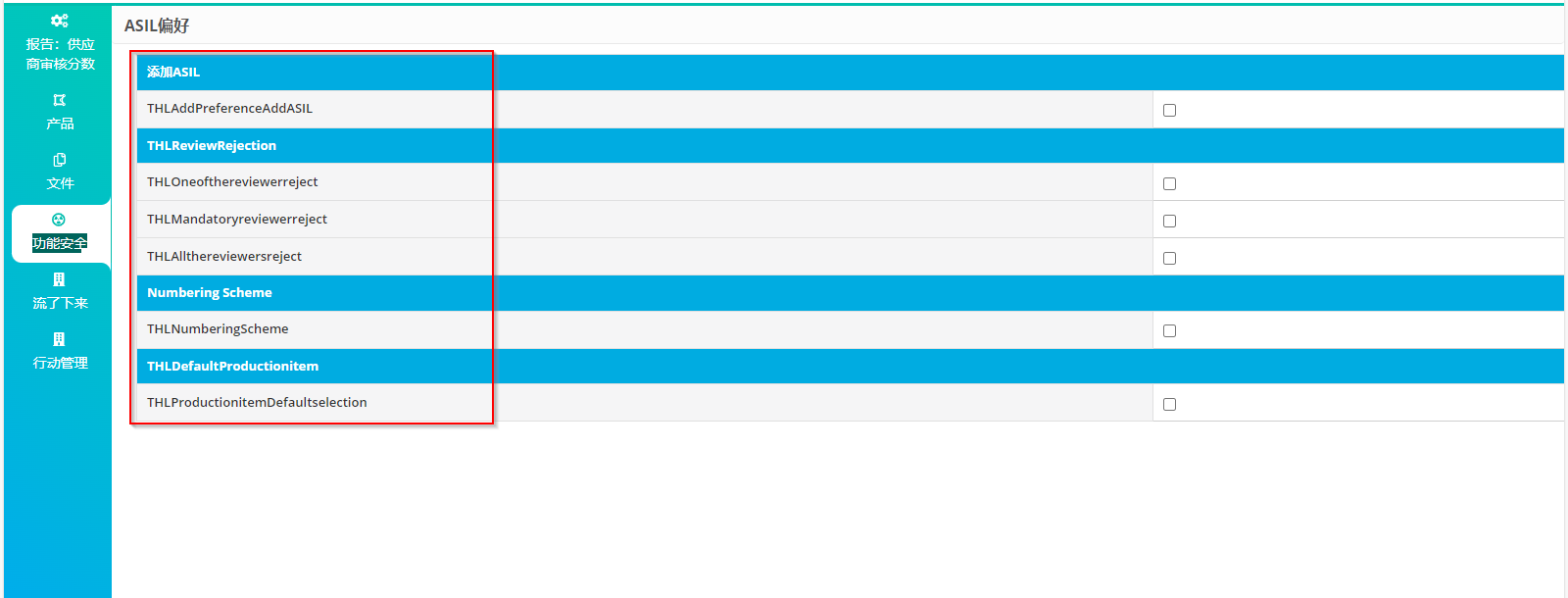
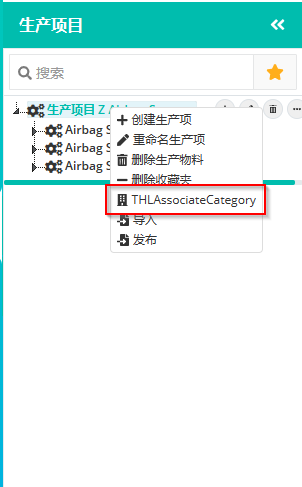
**1130 FST Chinese Language verification**

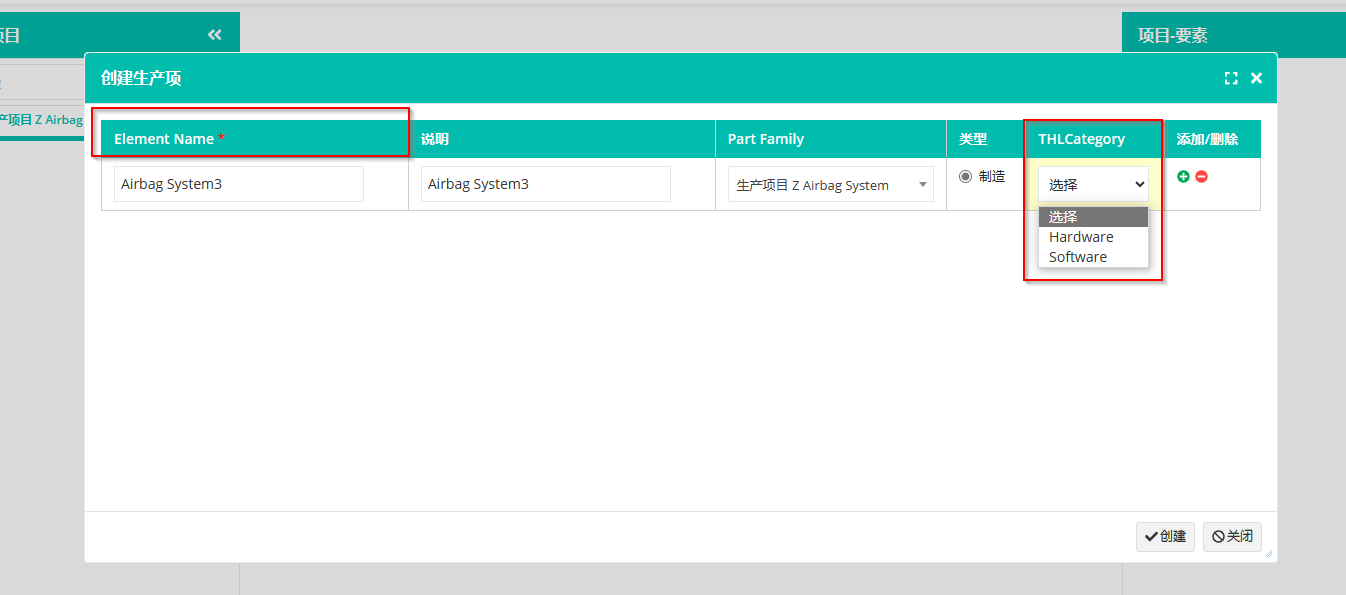
**Preference**

****

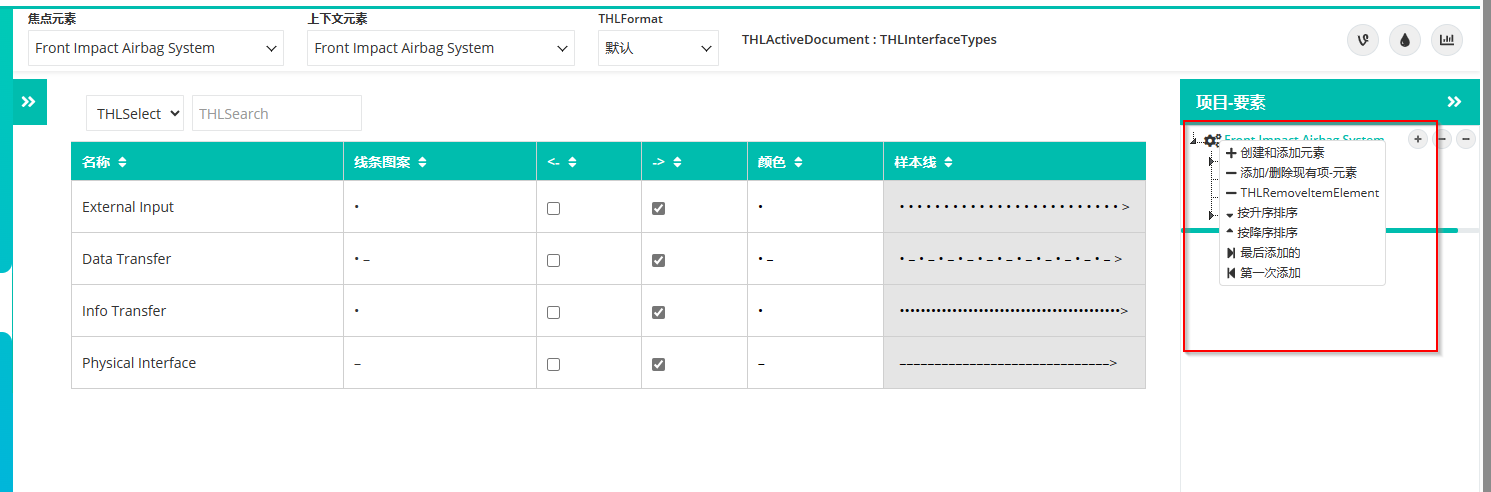
**Production Item Tree**

****

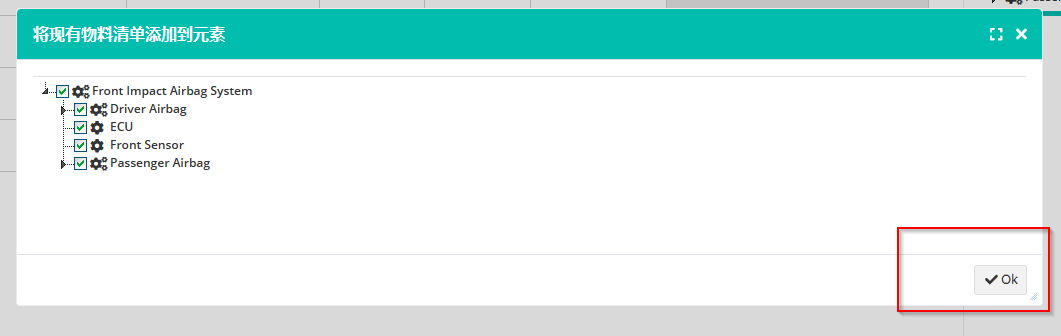
**Create PI**

****

**BOM Tree**

****

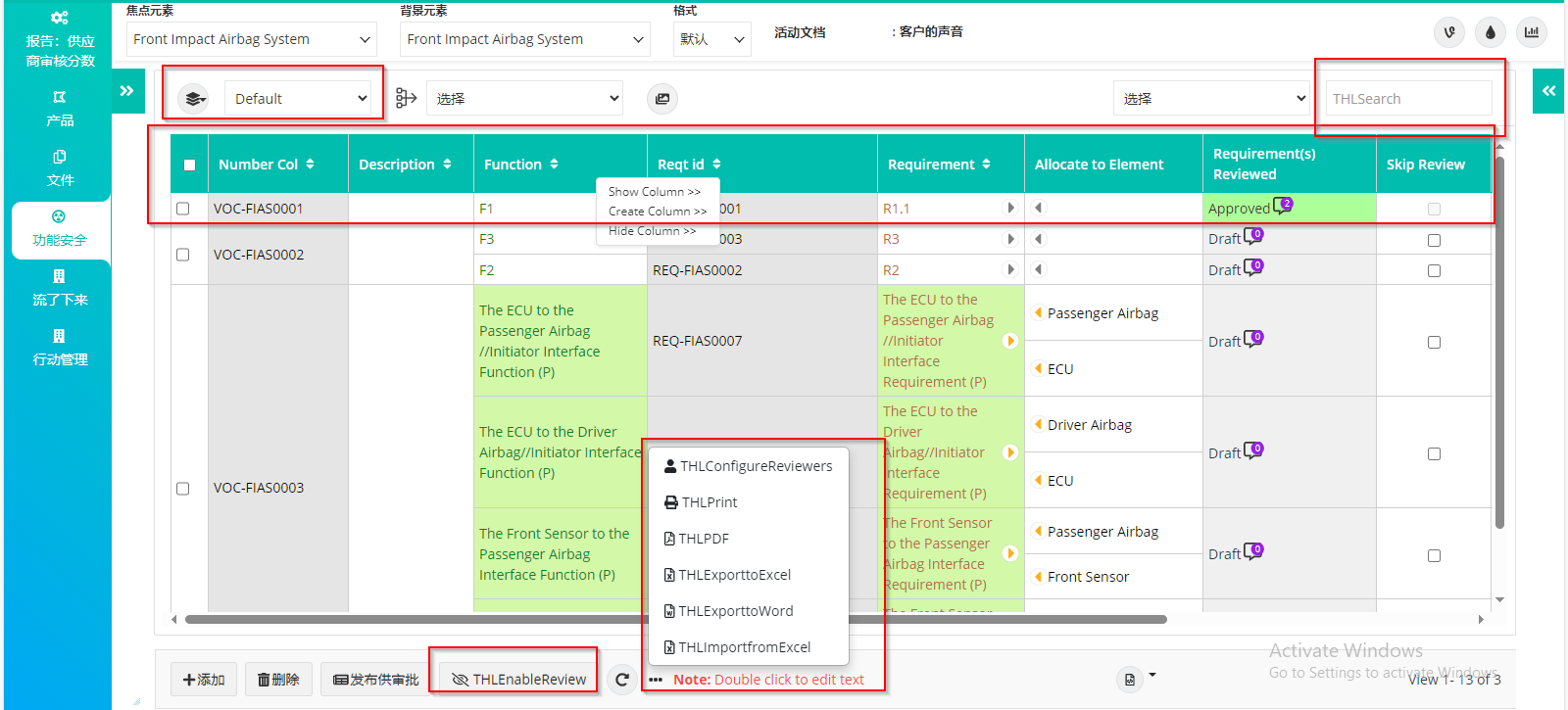
**Remove Existing Elements**

****

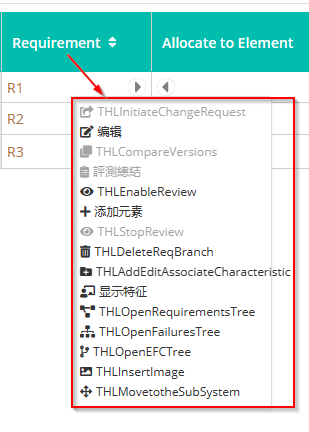
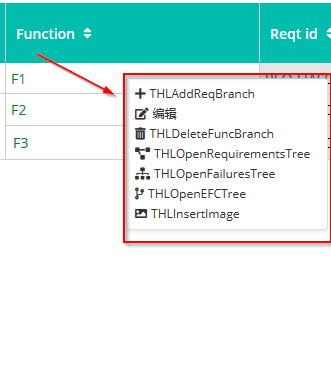
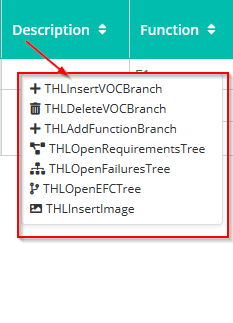
**Interface Types**

****

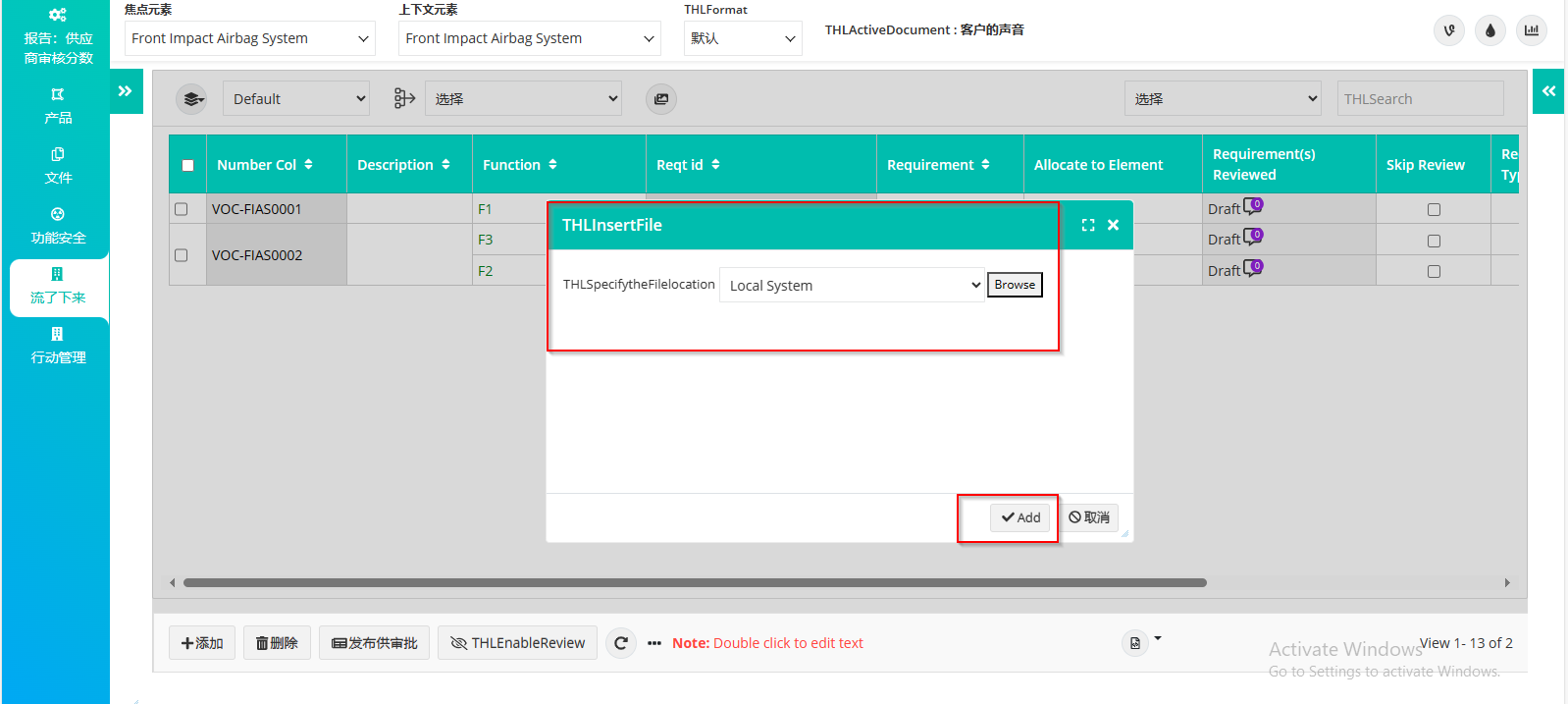
**Requirements Document**

****

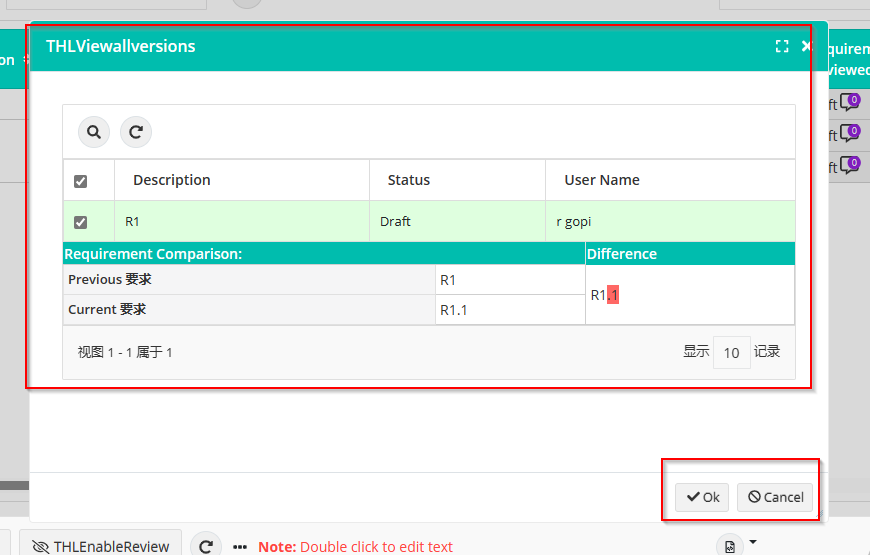
**Description Function Requirement**

****

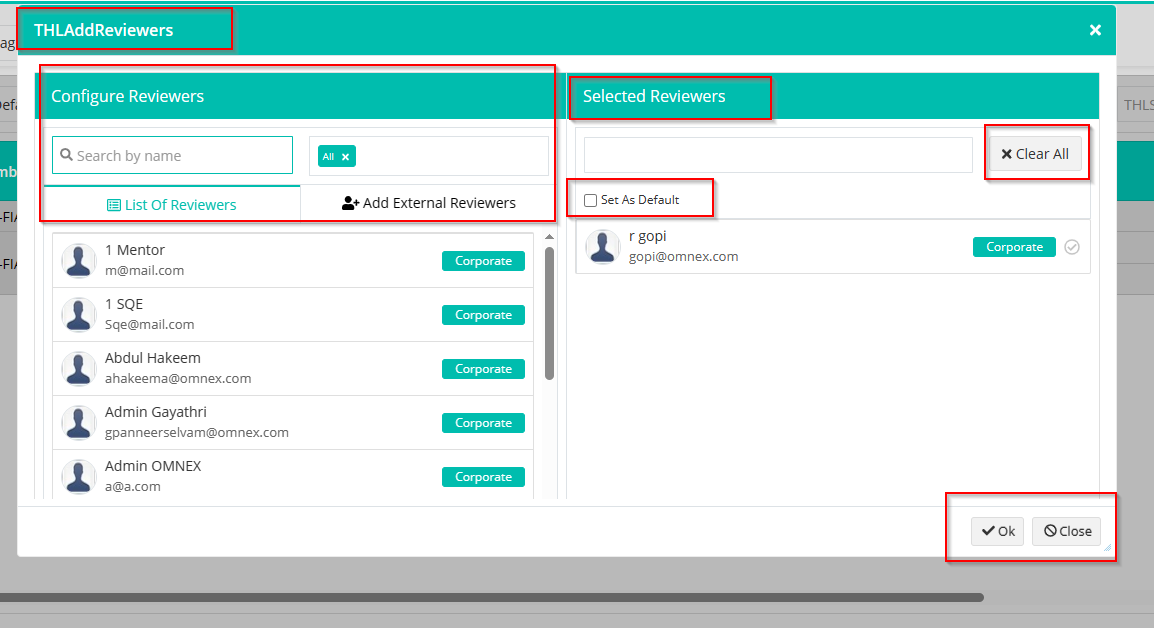
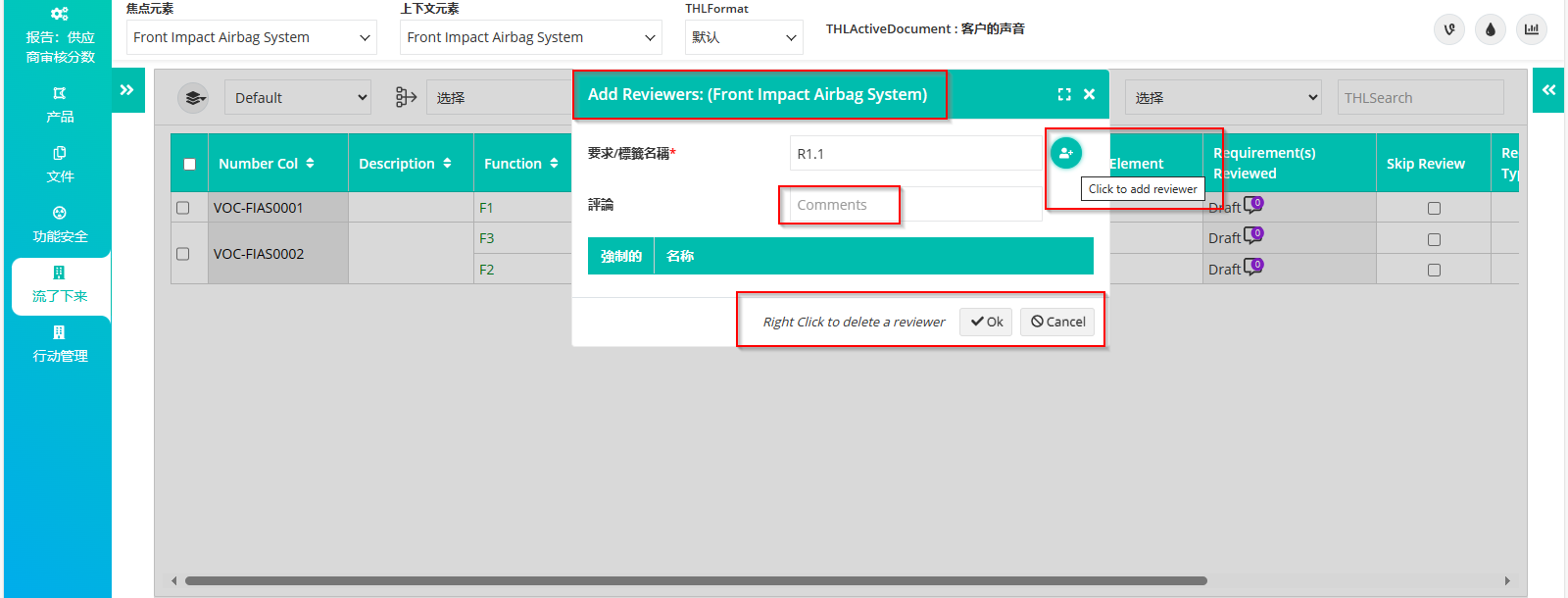
**Insert File**

****

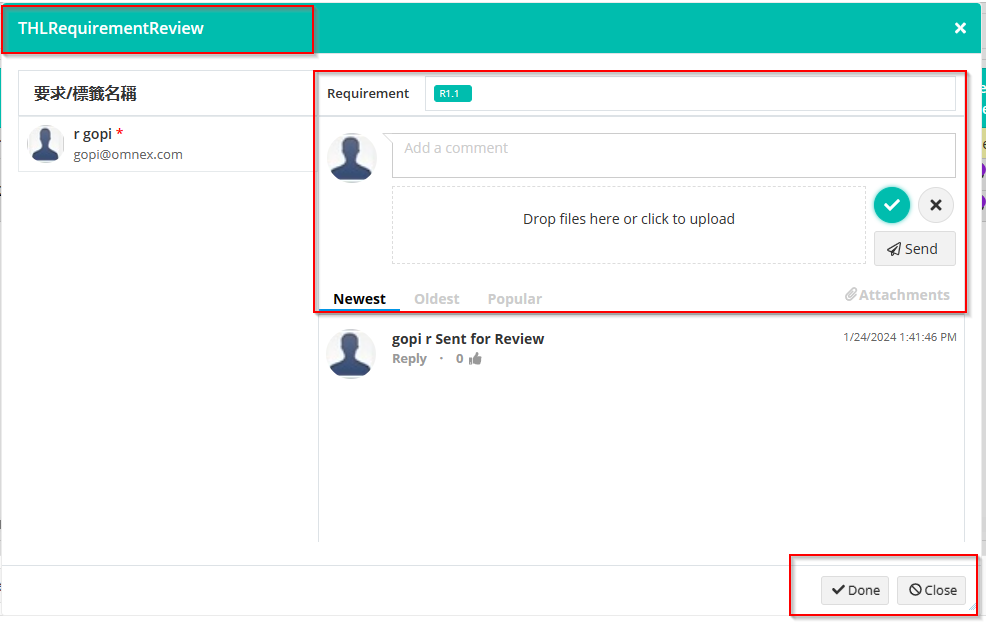
**Compare Version**

****

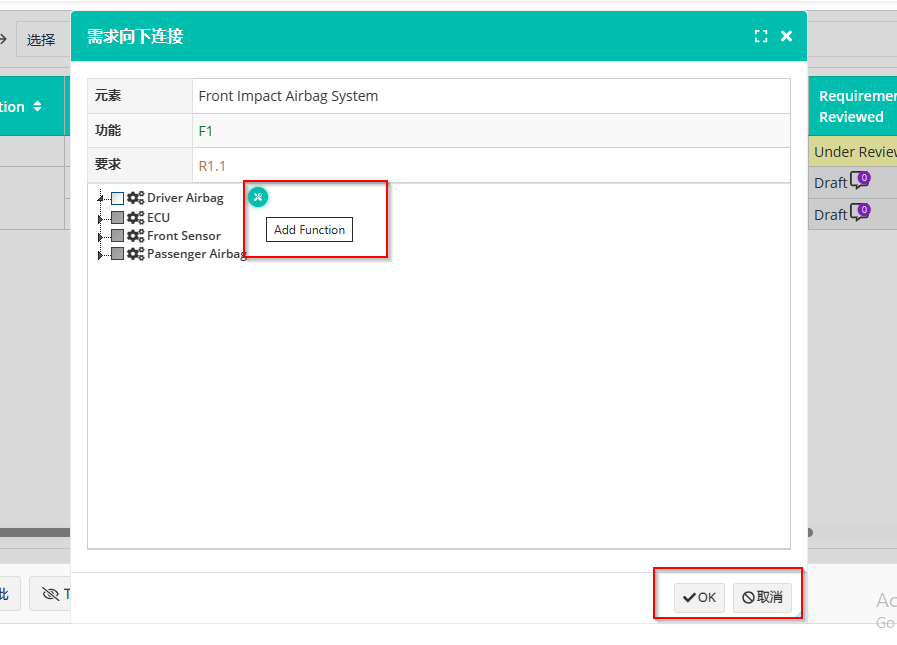
**Send For Review**

****

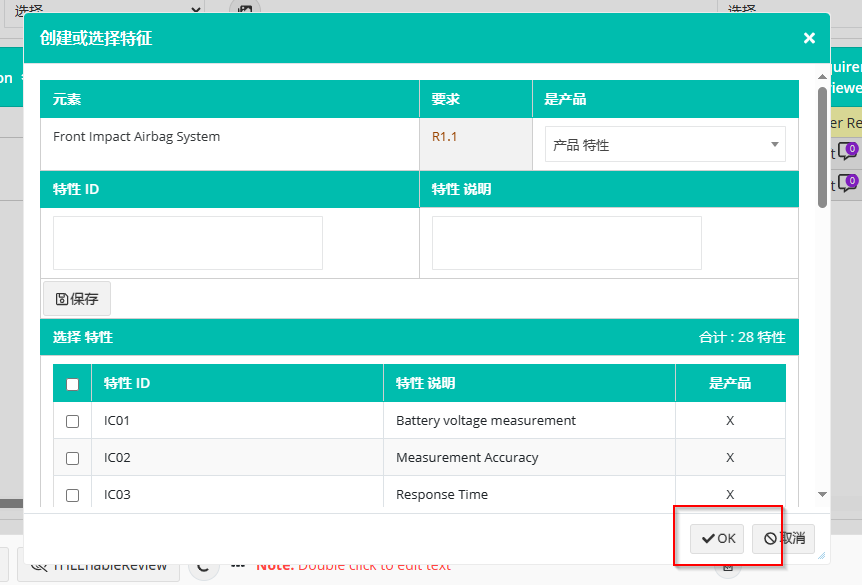
**Submit Review**

****

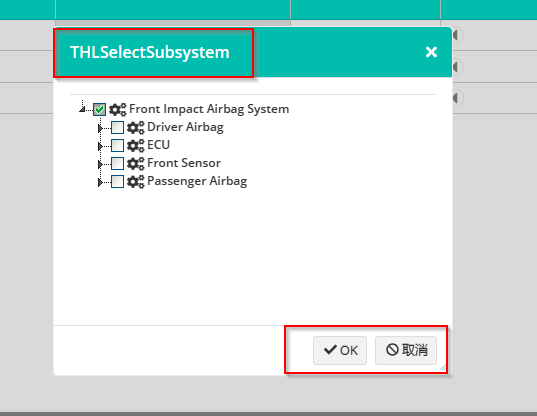
**Add Element**

****

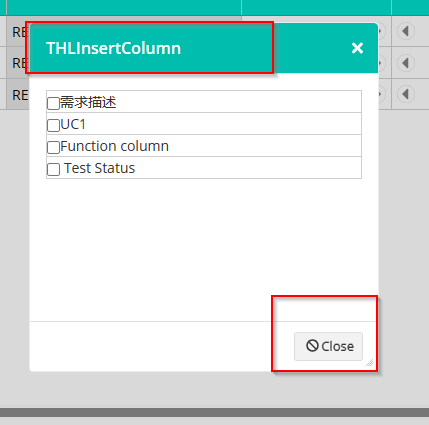
**Add Associate Characteristics**



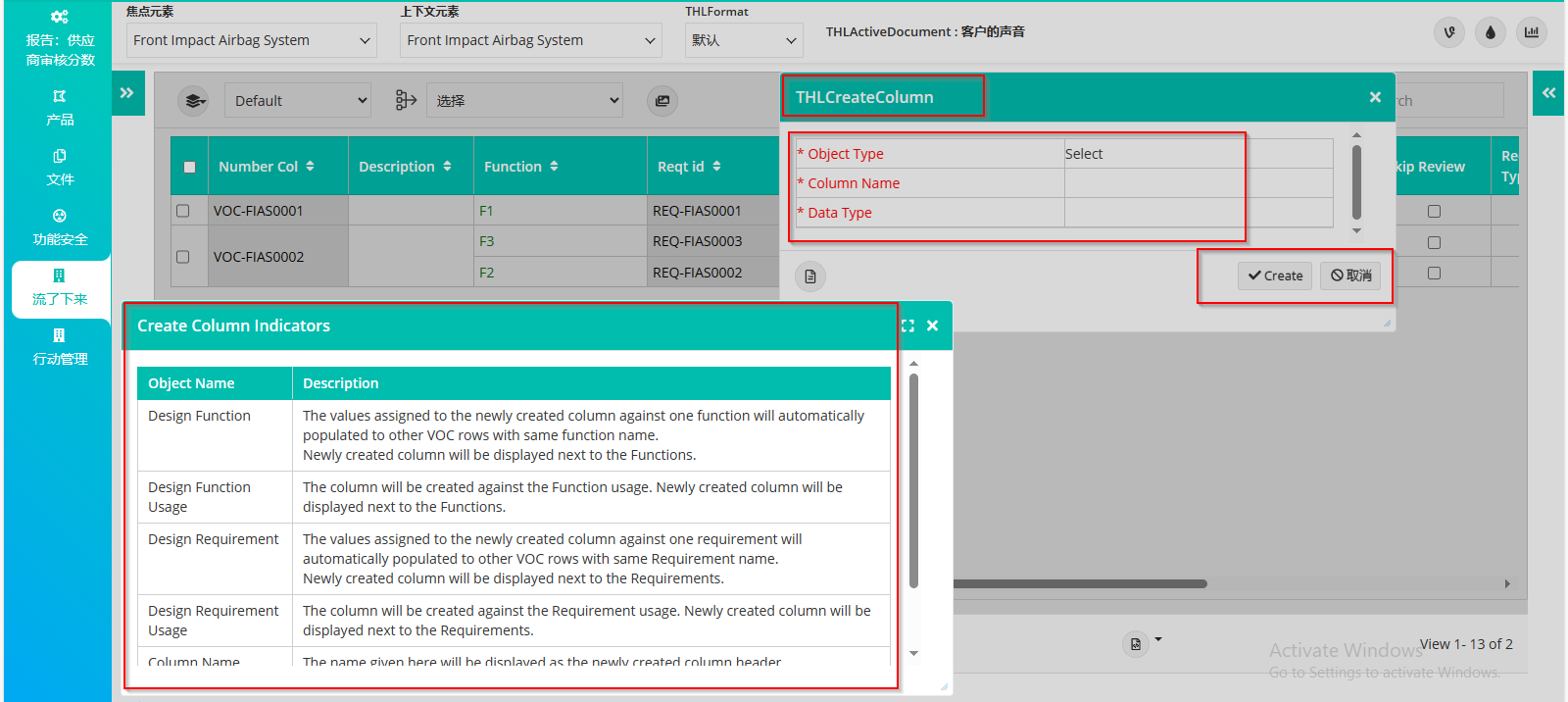
**Move to Sub-system**

****

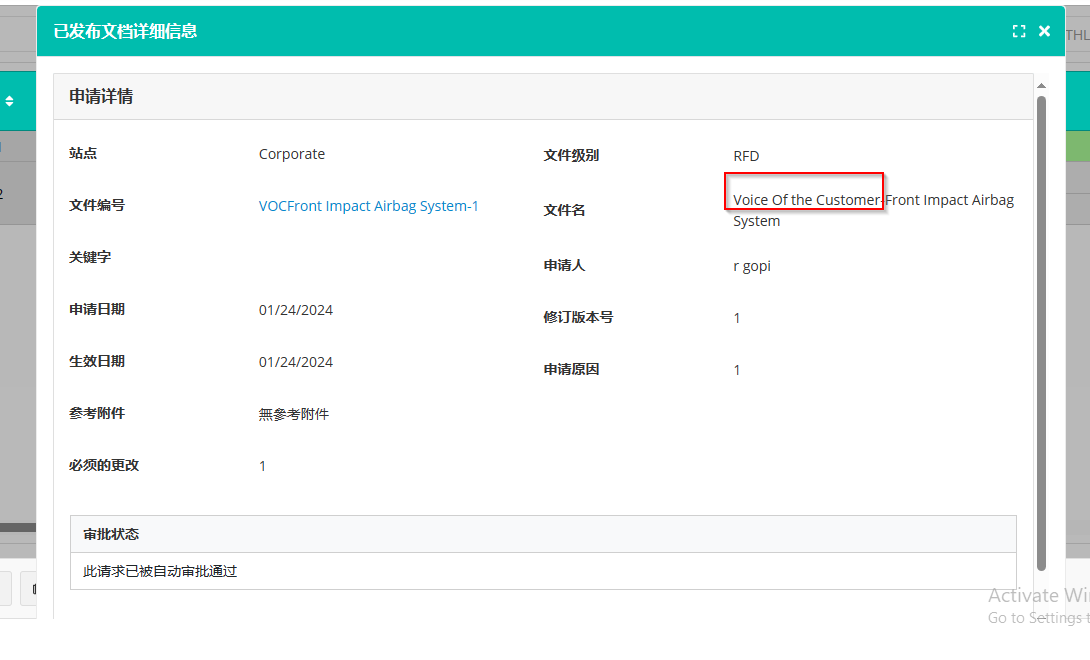
**Insert Column**

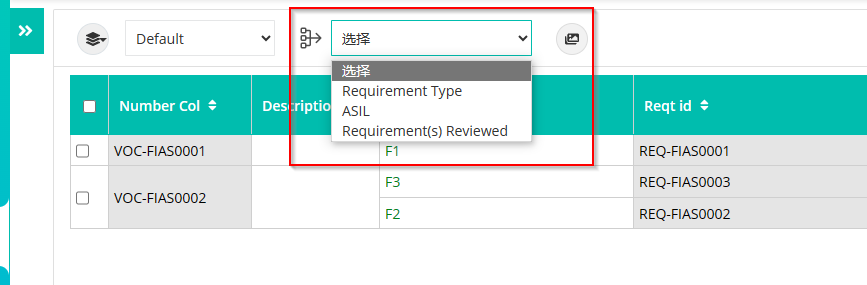
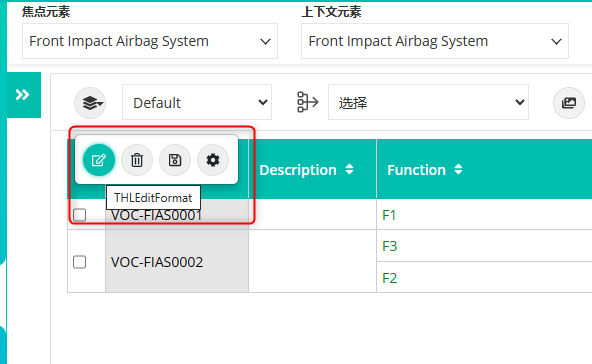
****

**Create column**

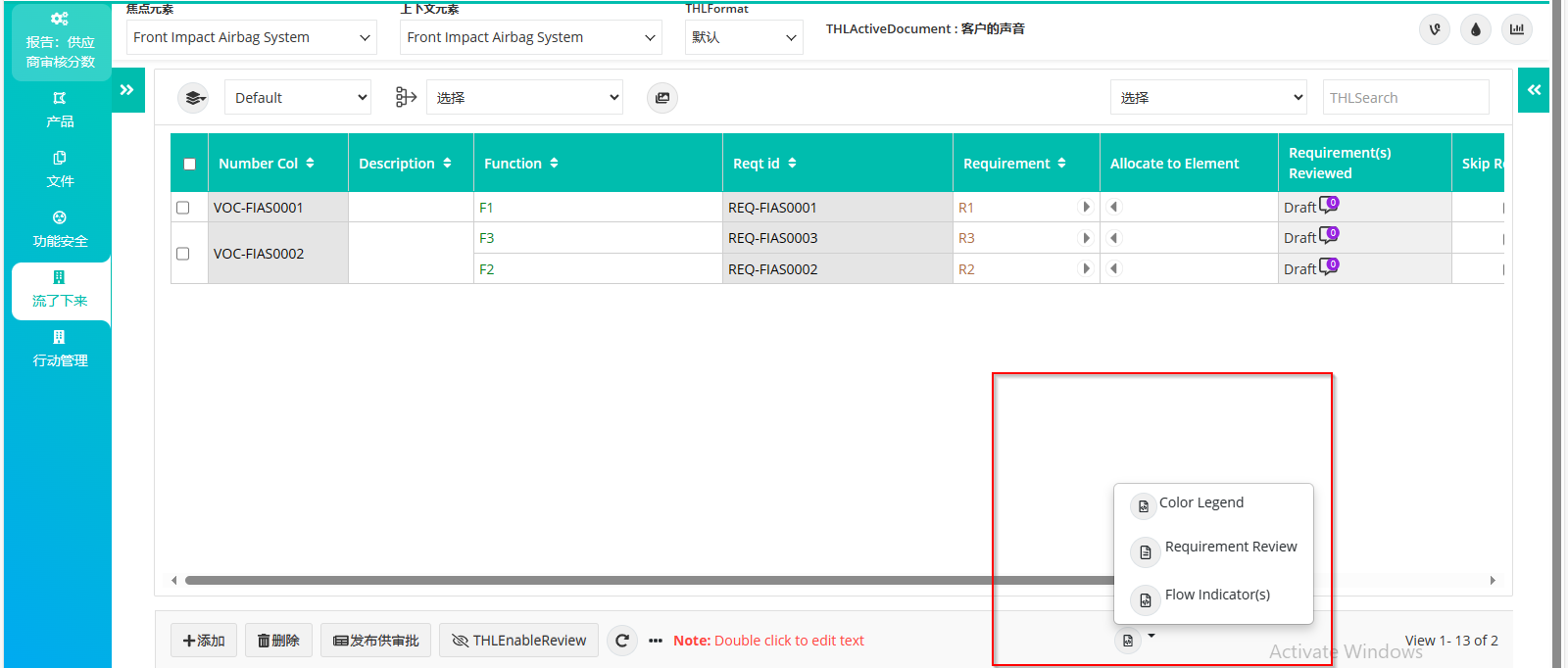
****

**Published Document**

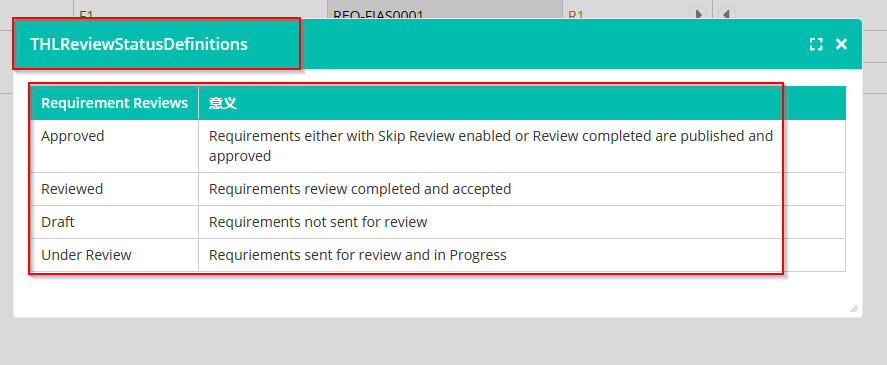
****

****

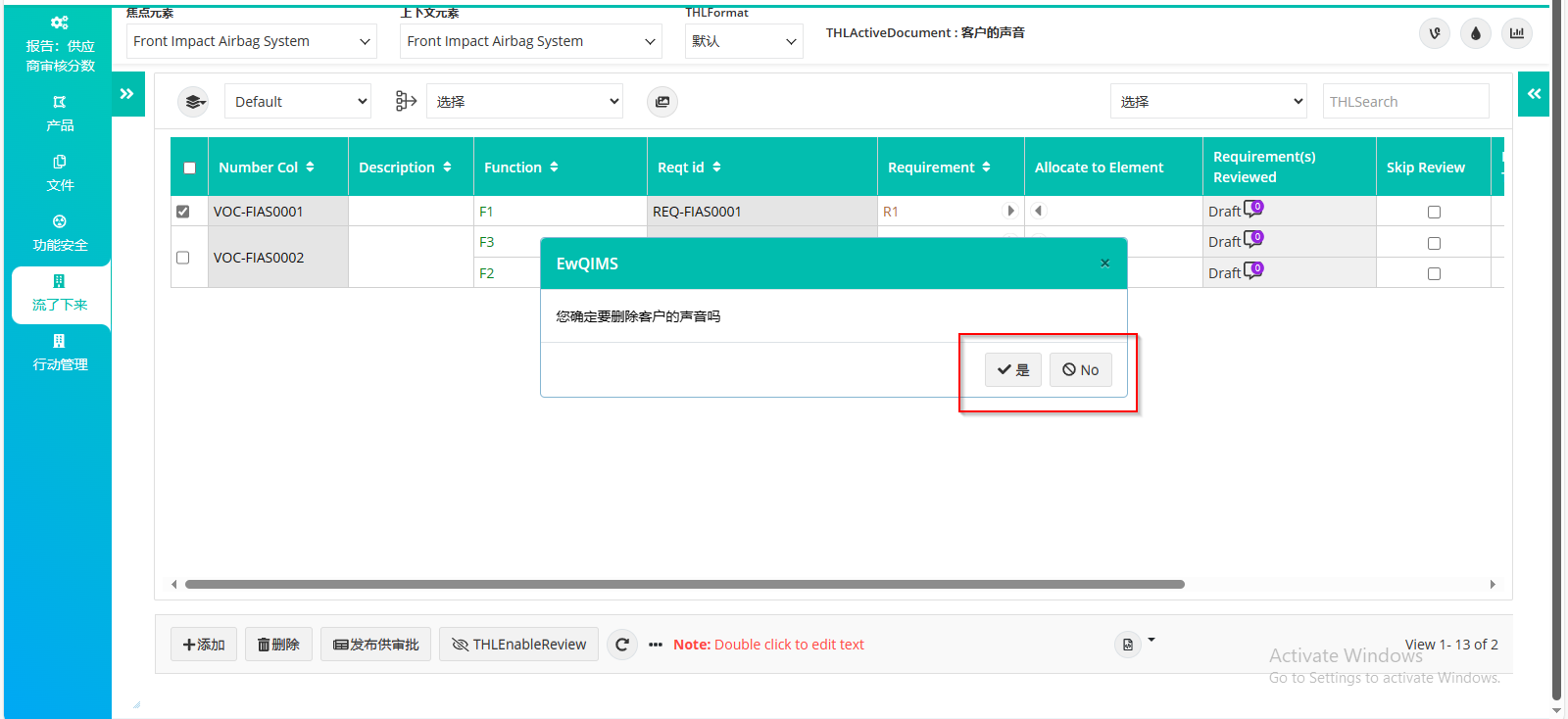
**Legends**

****

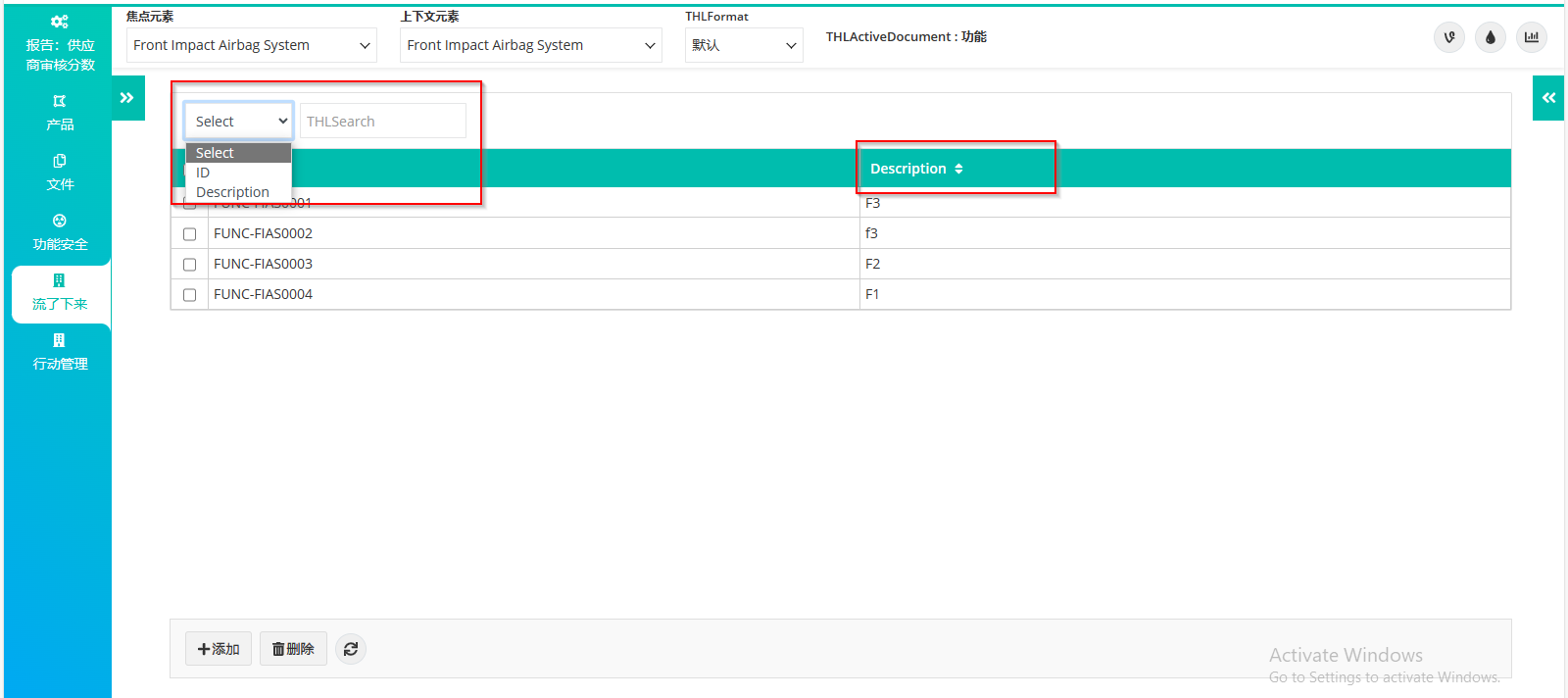
****

****

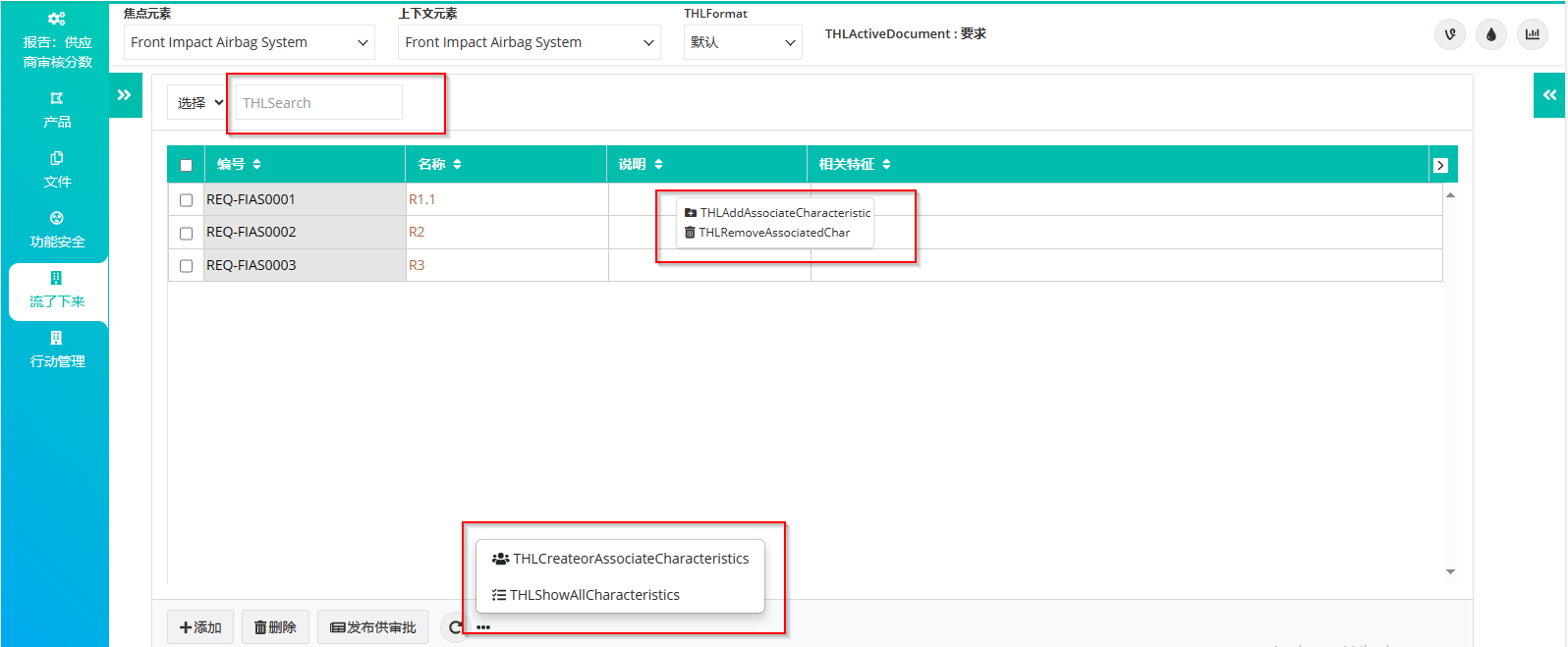
**Delete VOC**

****

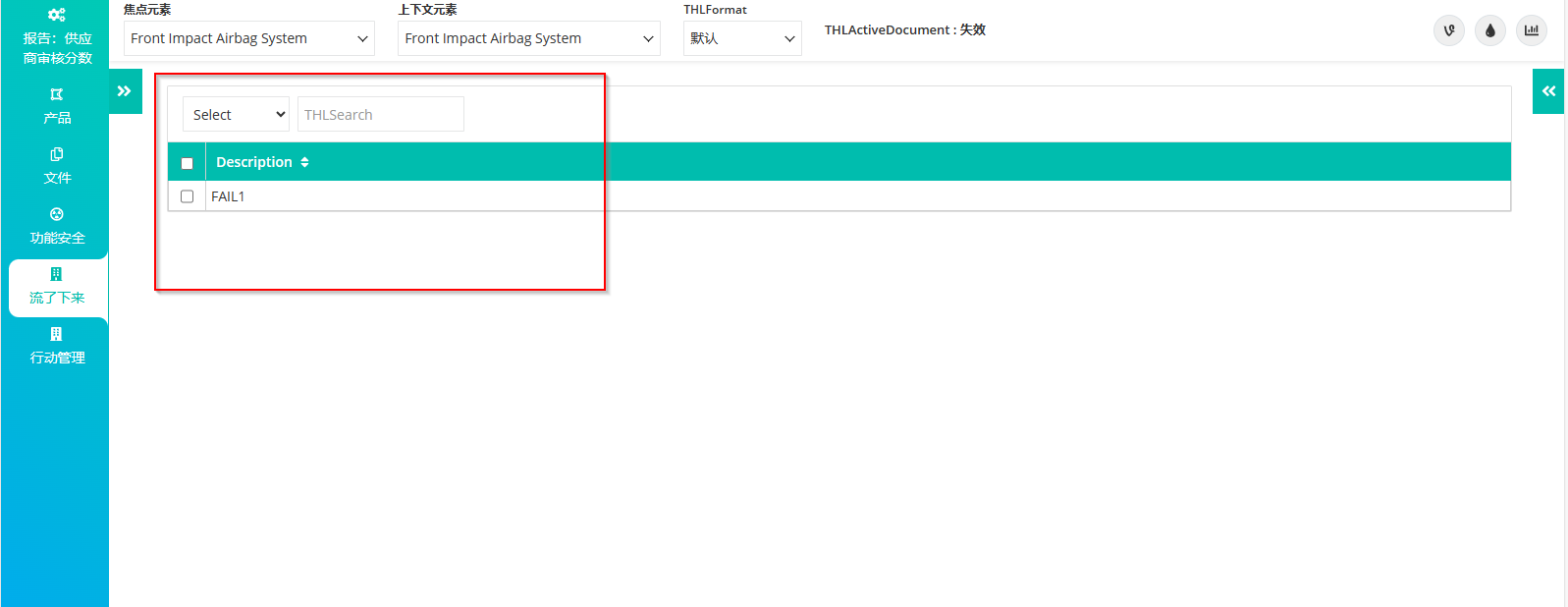
**Functions**

****

**Requirements**

****

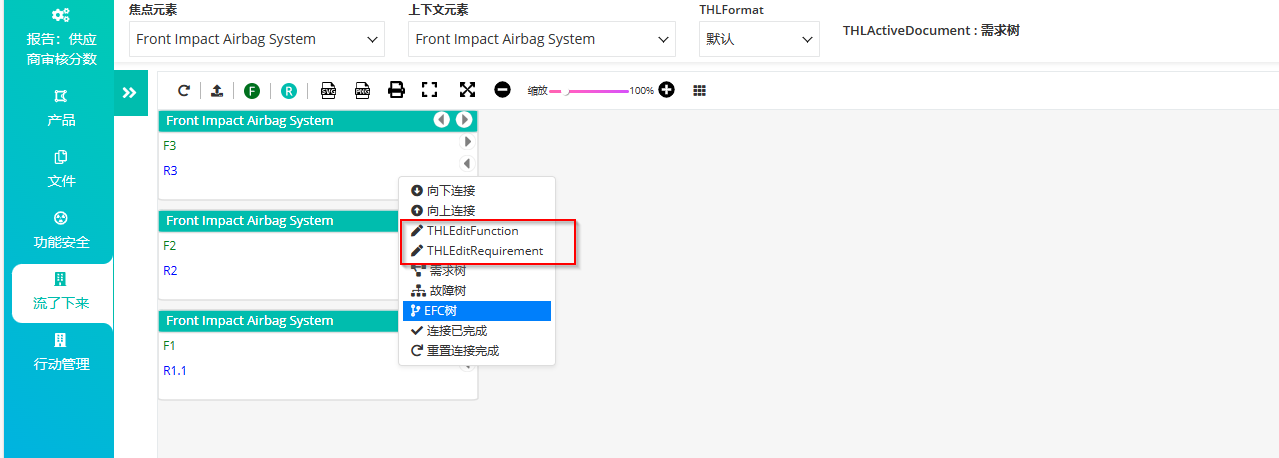
**Failures**

****

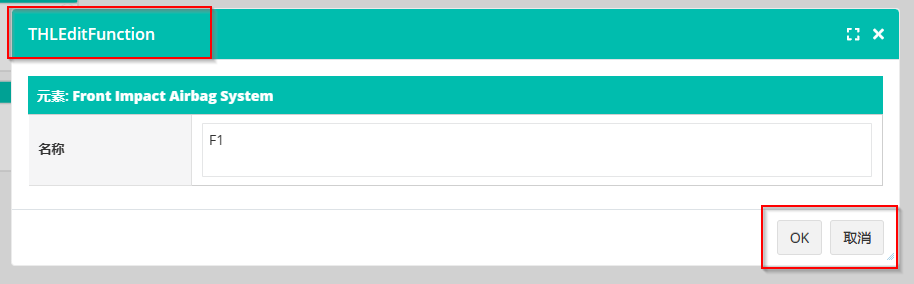
**Alert**

****

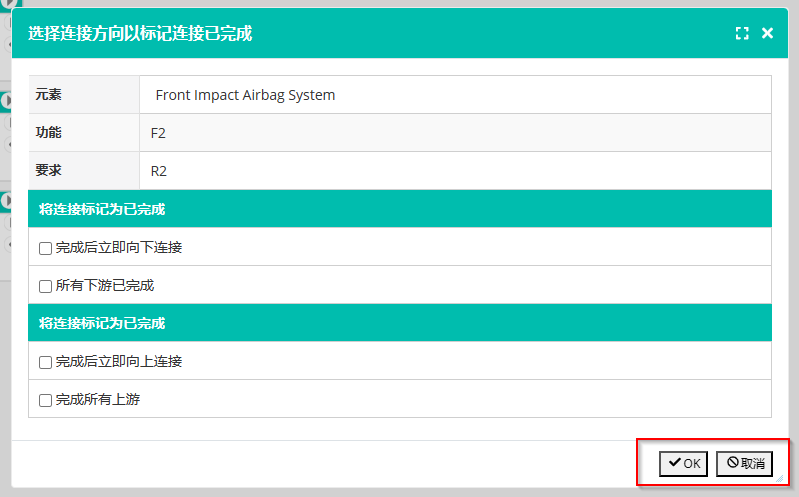
**Requirements Tree**

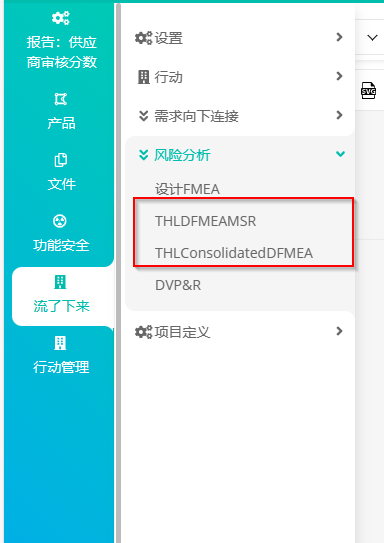
****

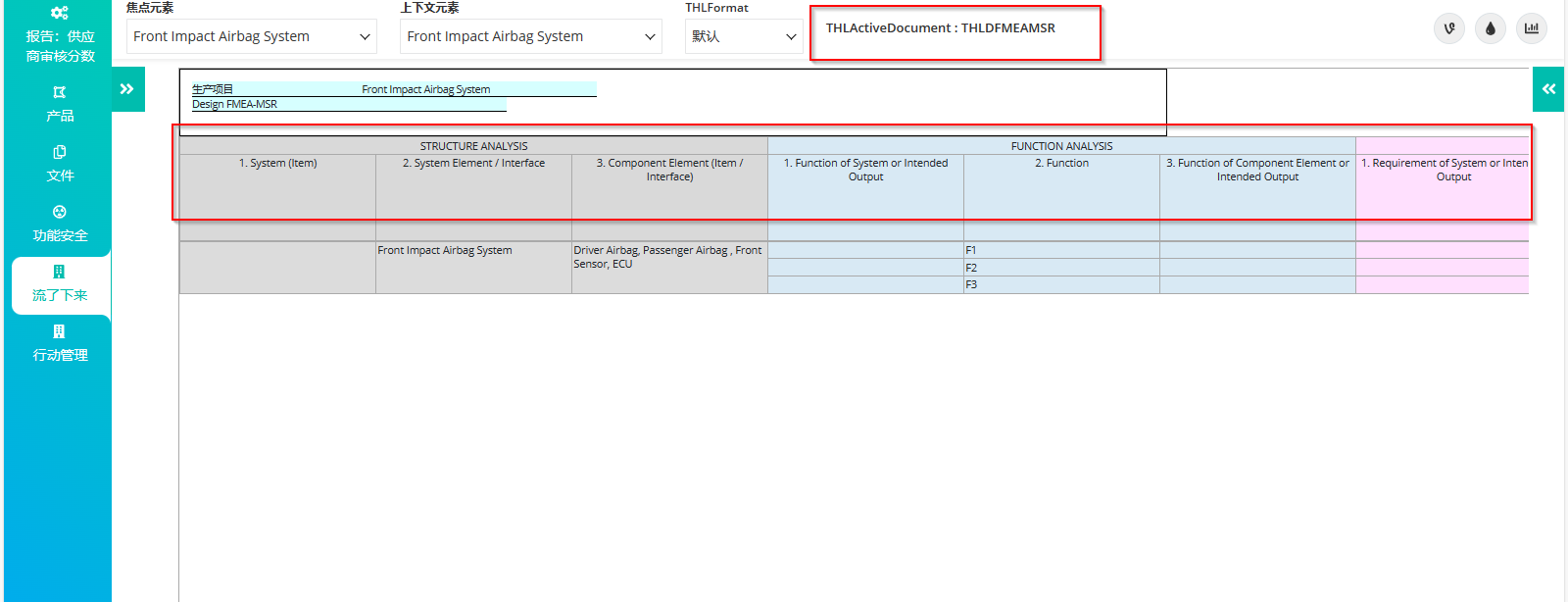
**Edit Function**

****

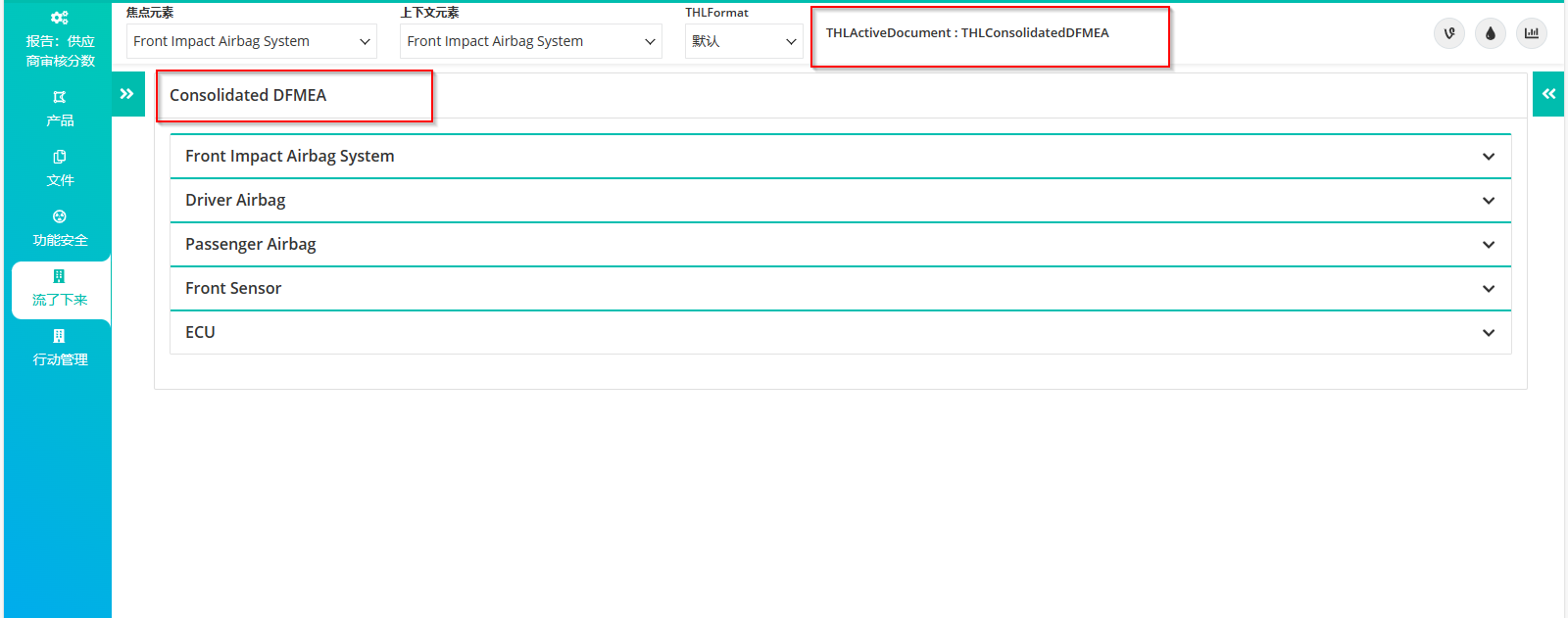
**Flows Done & Rest Flows Done**

****

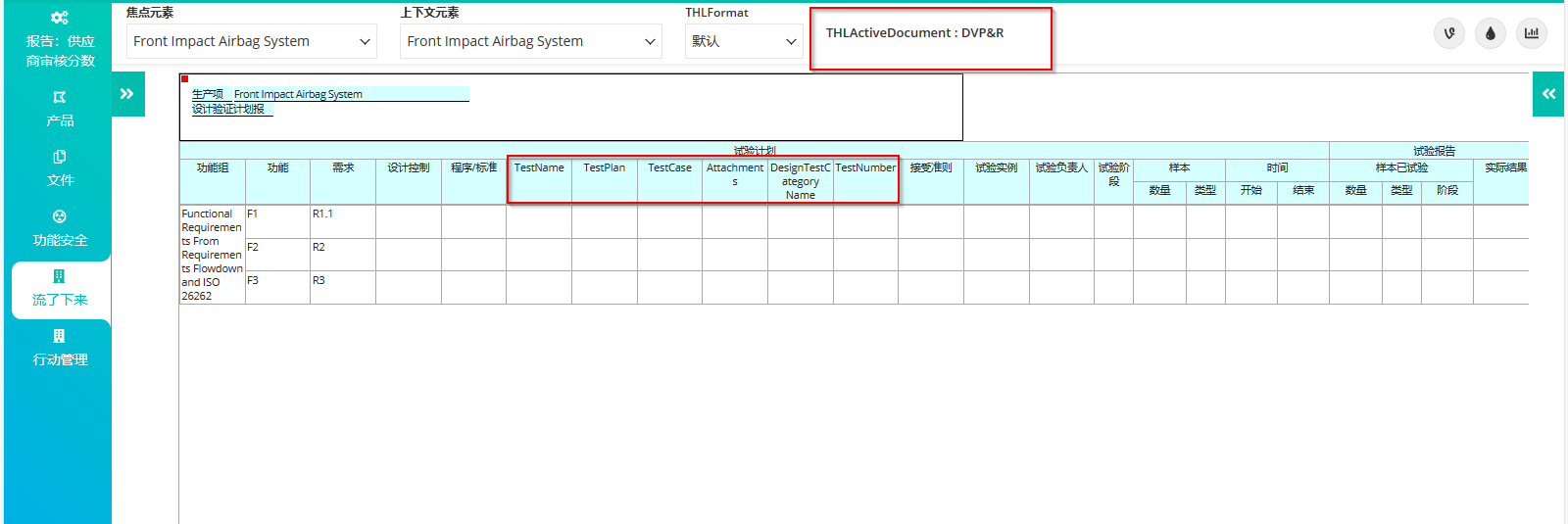
****

****

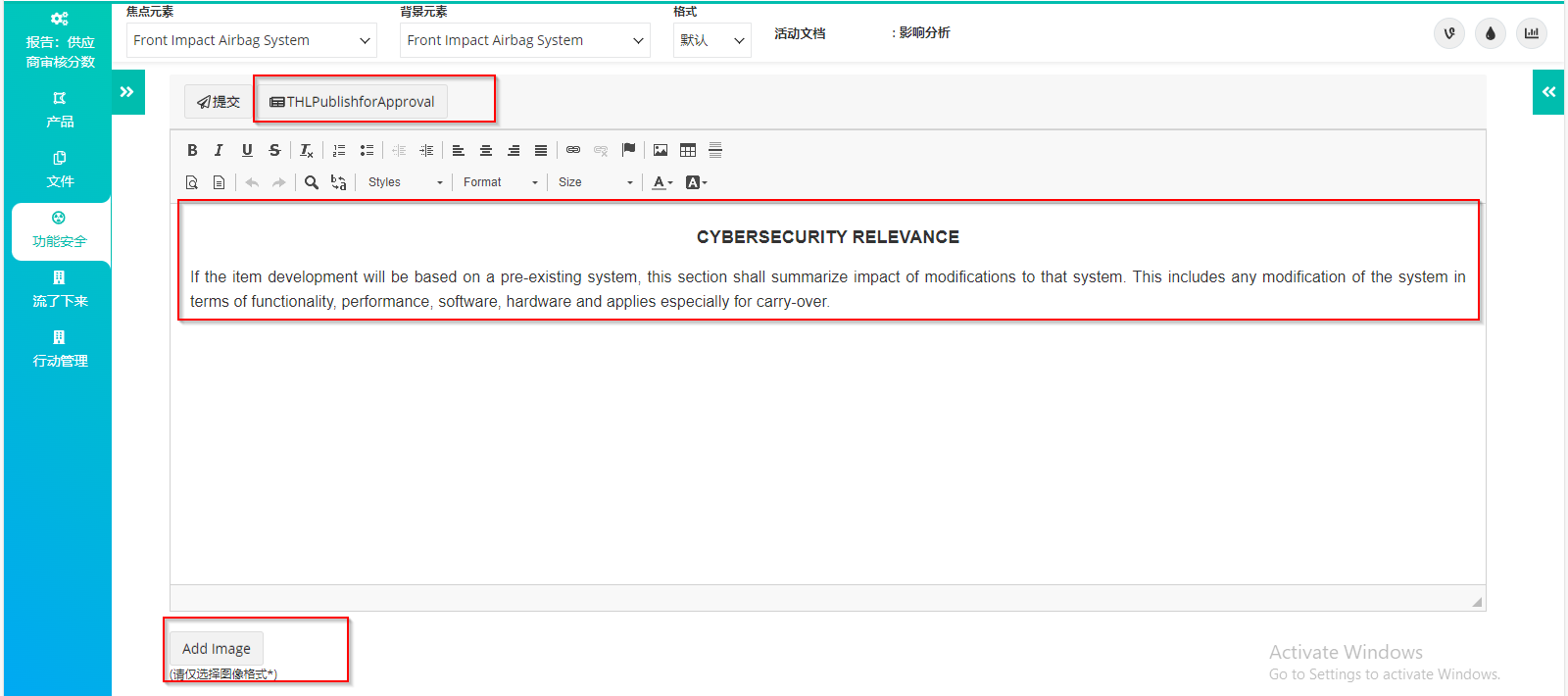
**Consolidated DFMEA**

****

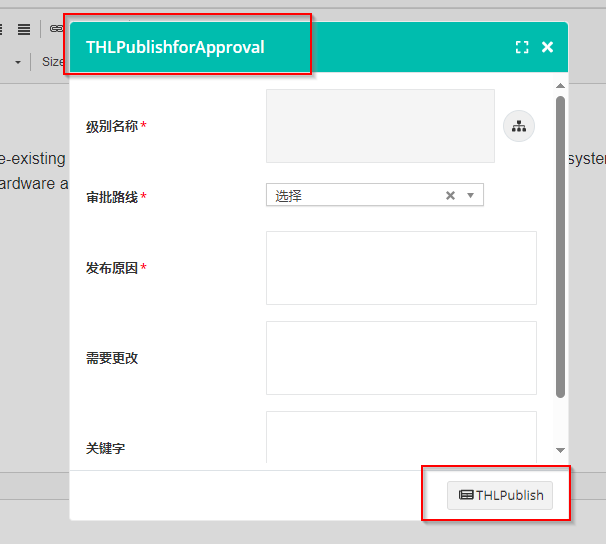
**DVP&R**

****

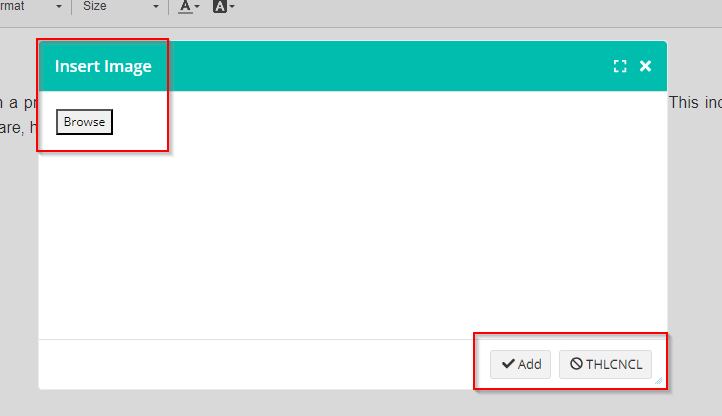
**Impact Analysis**

****

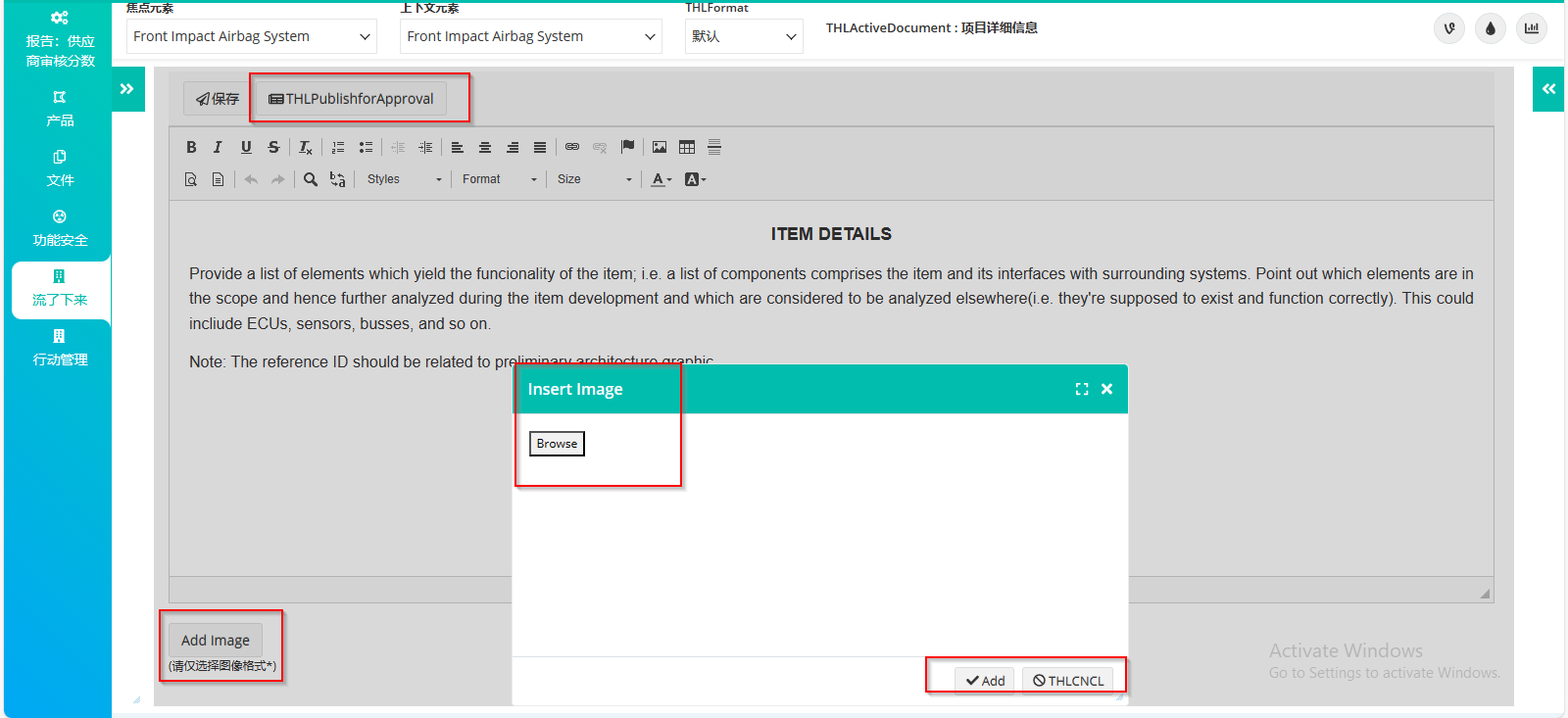
**Publish for approval**

****

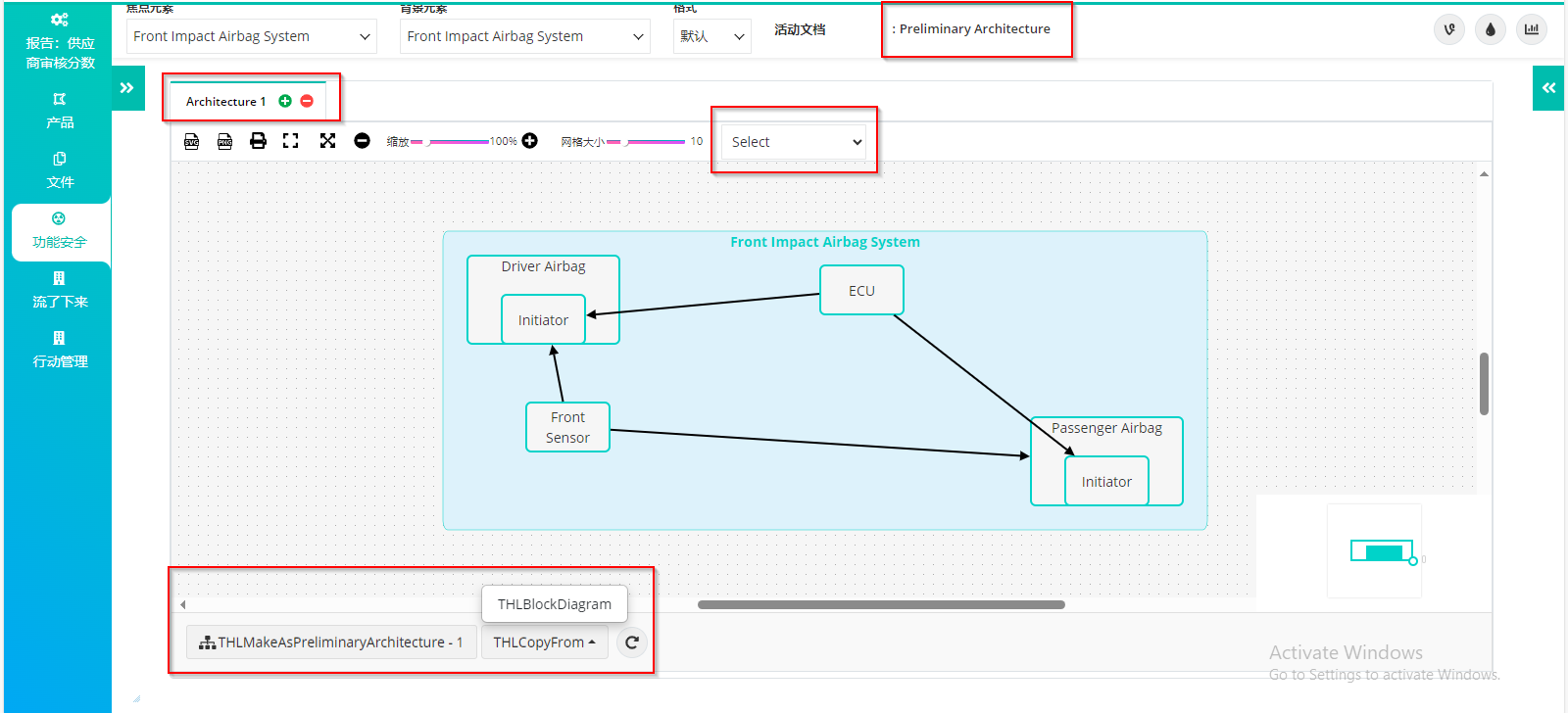
**Insert Image**

****

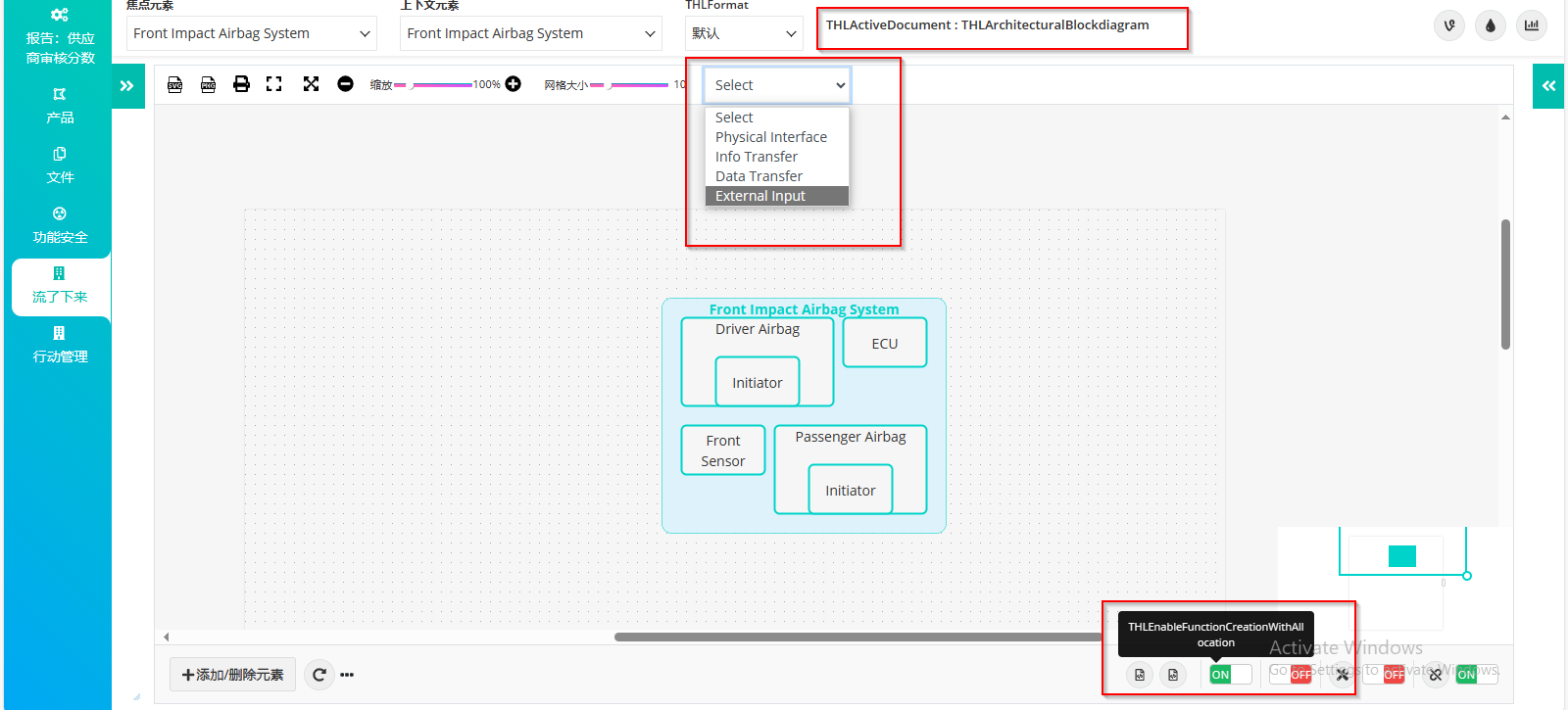
**Item Details**

****

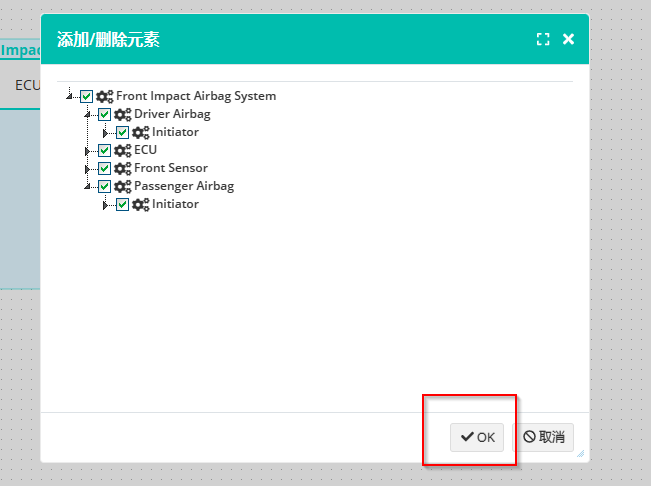
**Preliminary Architecture**

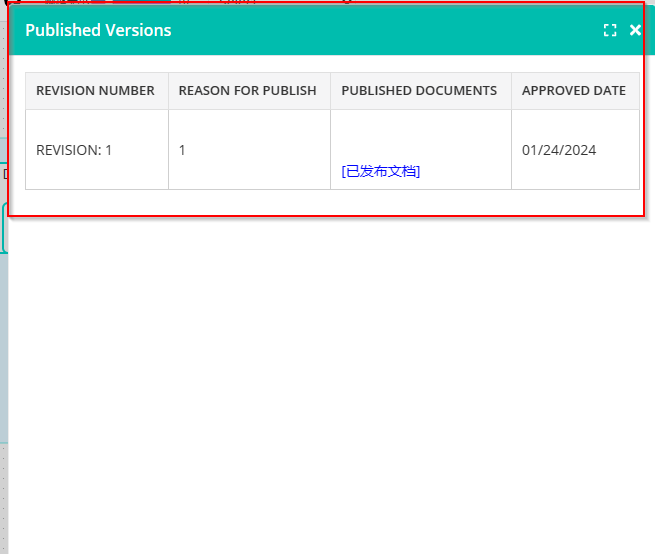
****

**Block Diagram**

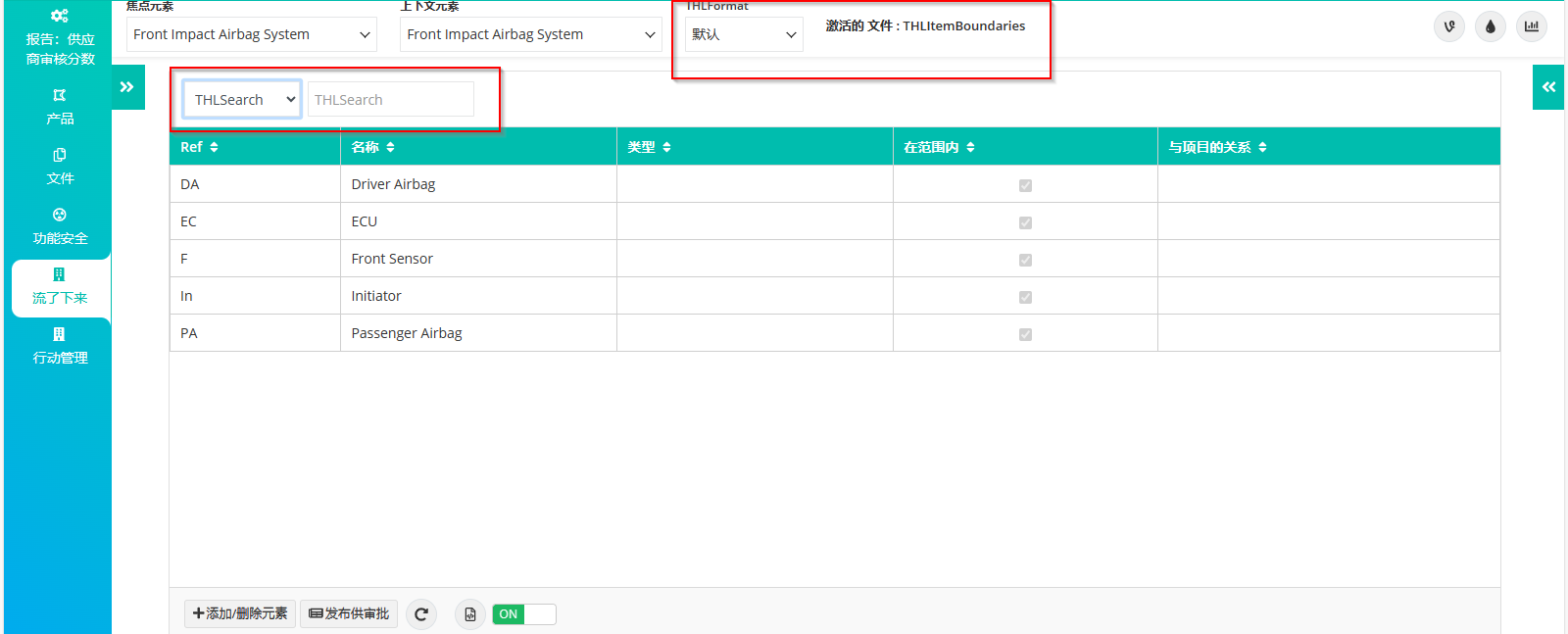
****

**Add/Remove Elements**

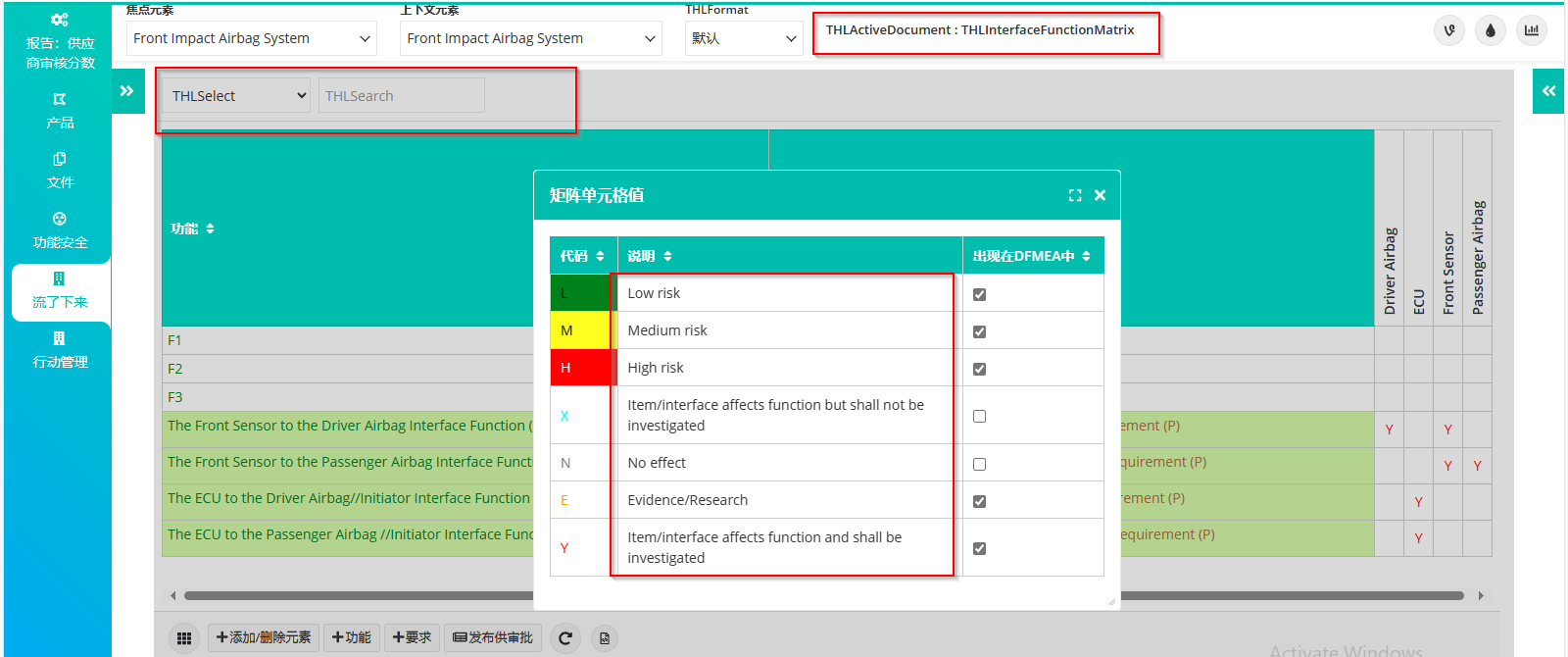
****

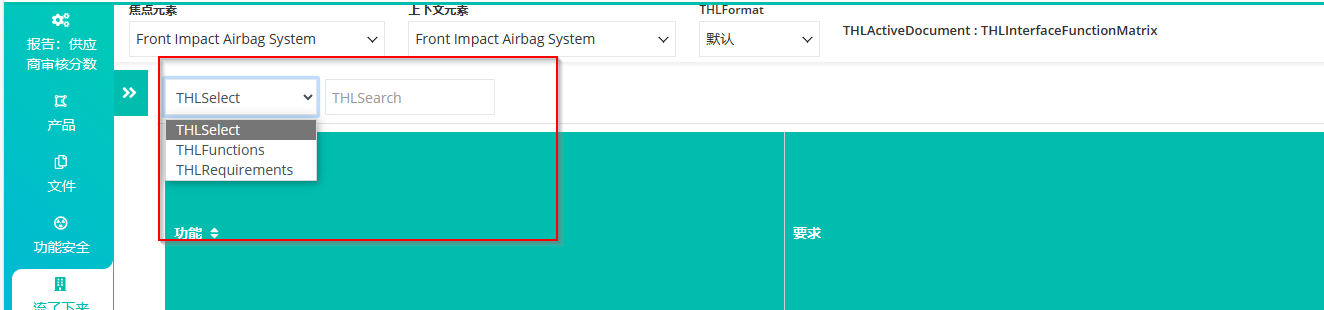
****

**Item Boundaries**

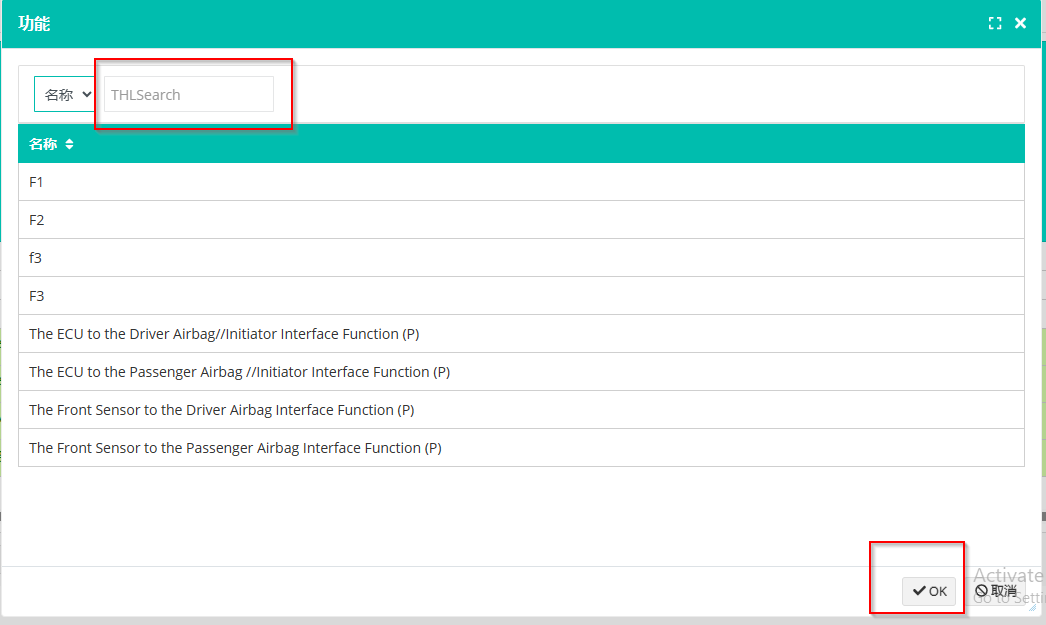
****

**IFM**

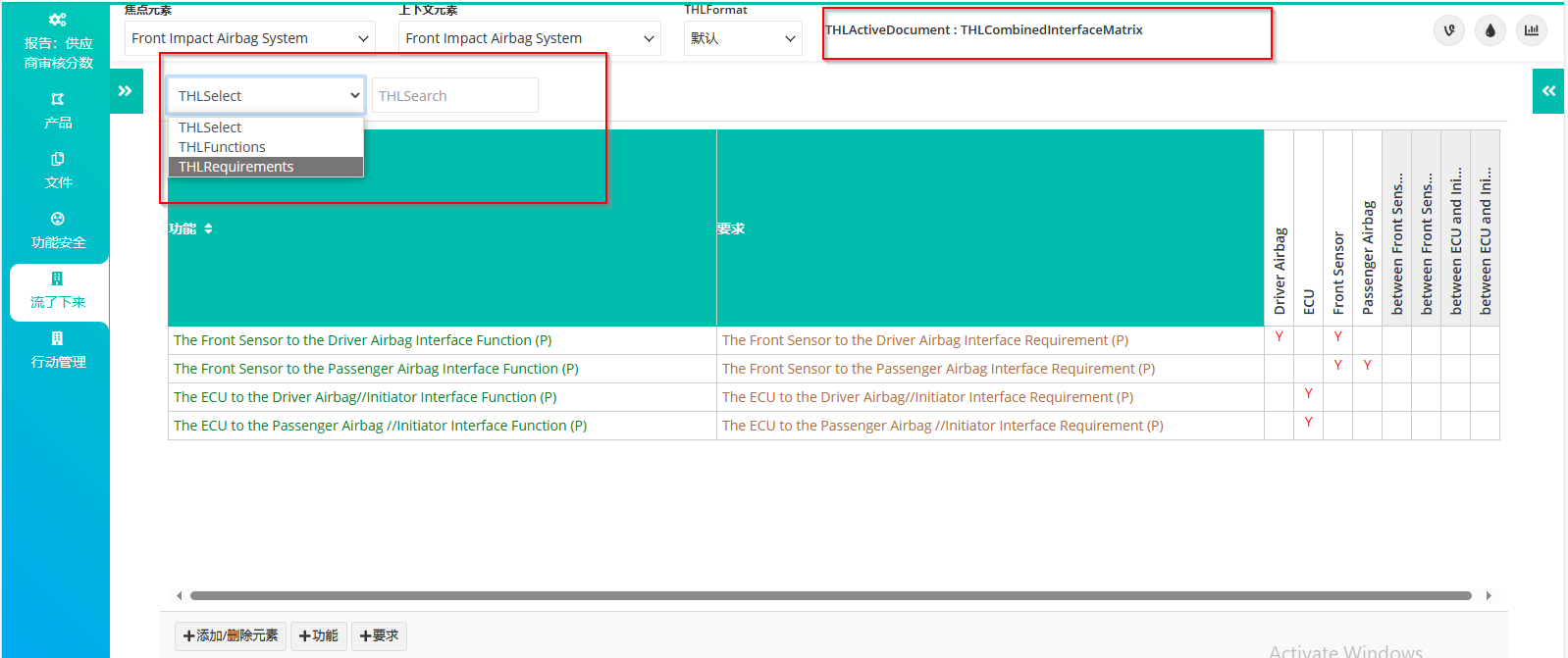
****

****

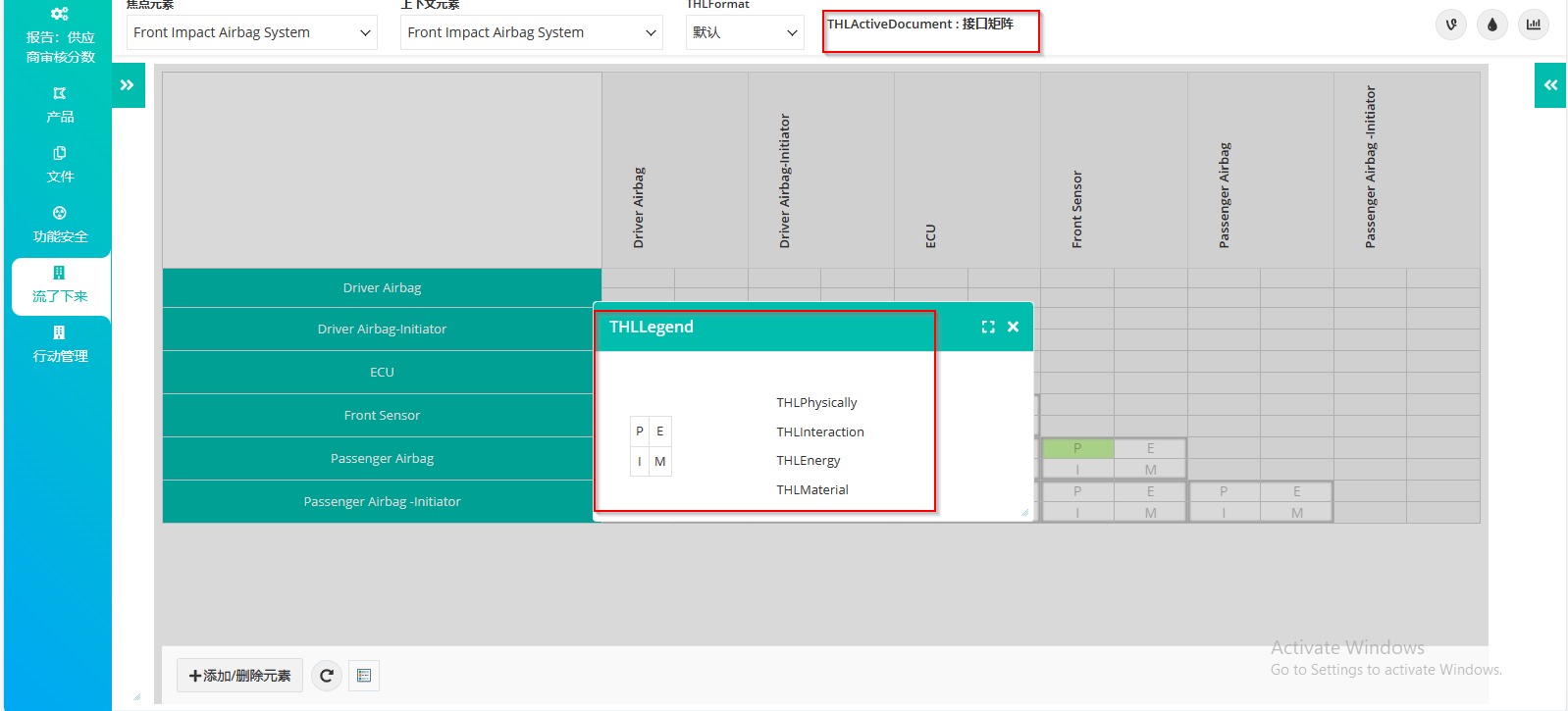
**+Functions and +Requirements**

****

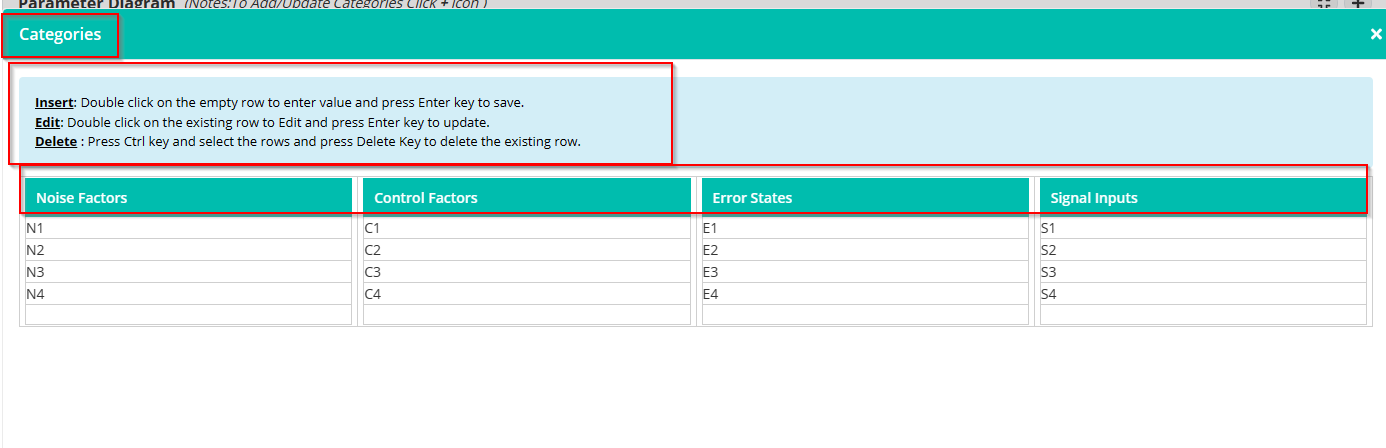
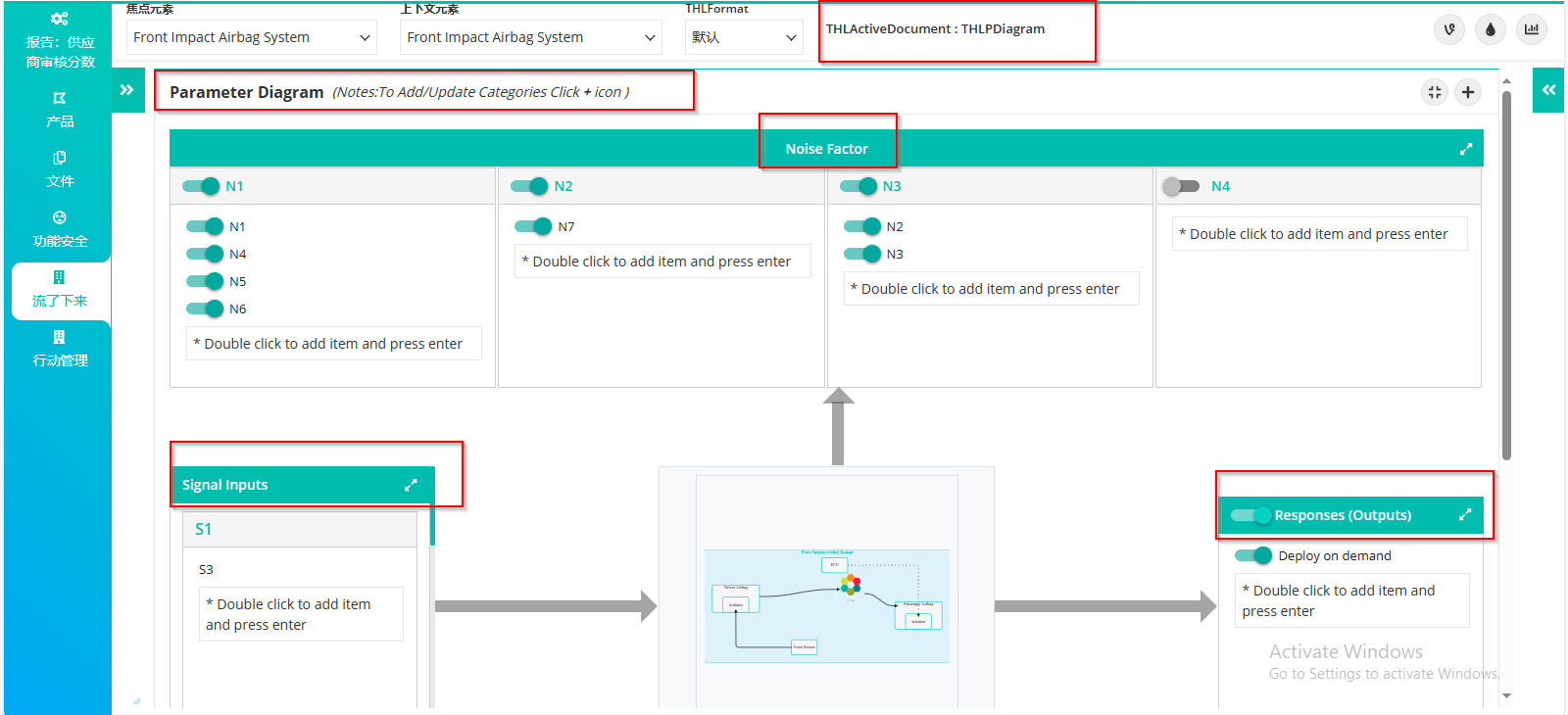
**Combined Interface Matrix**

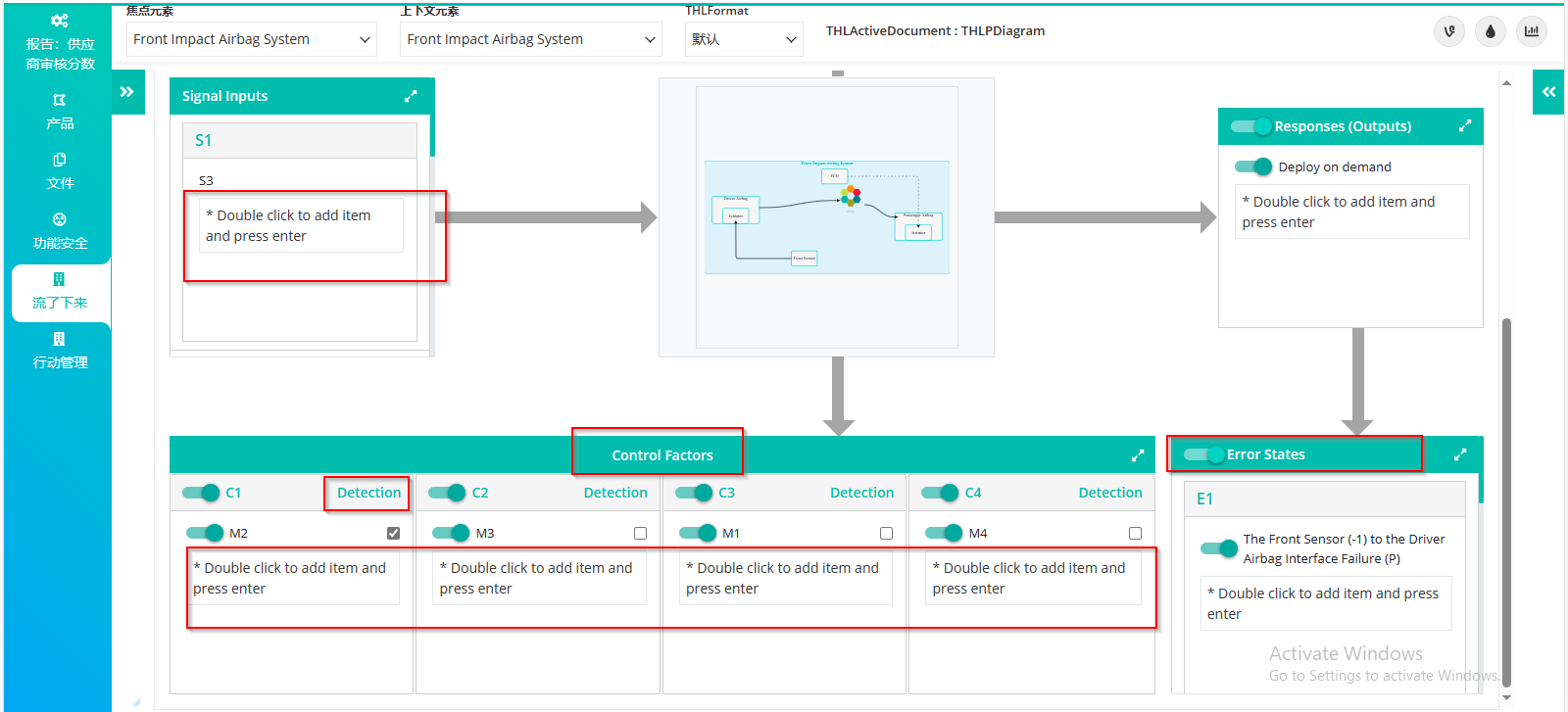
****

**Interface Matrix**

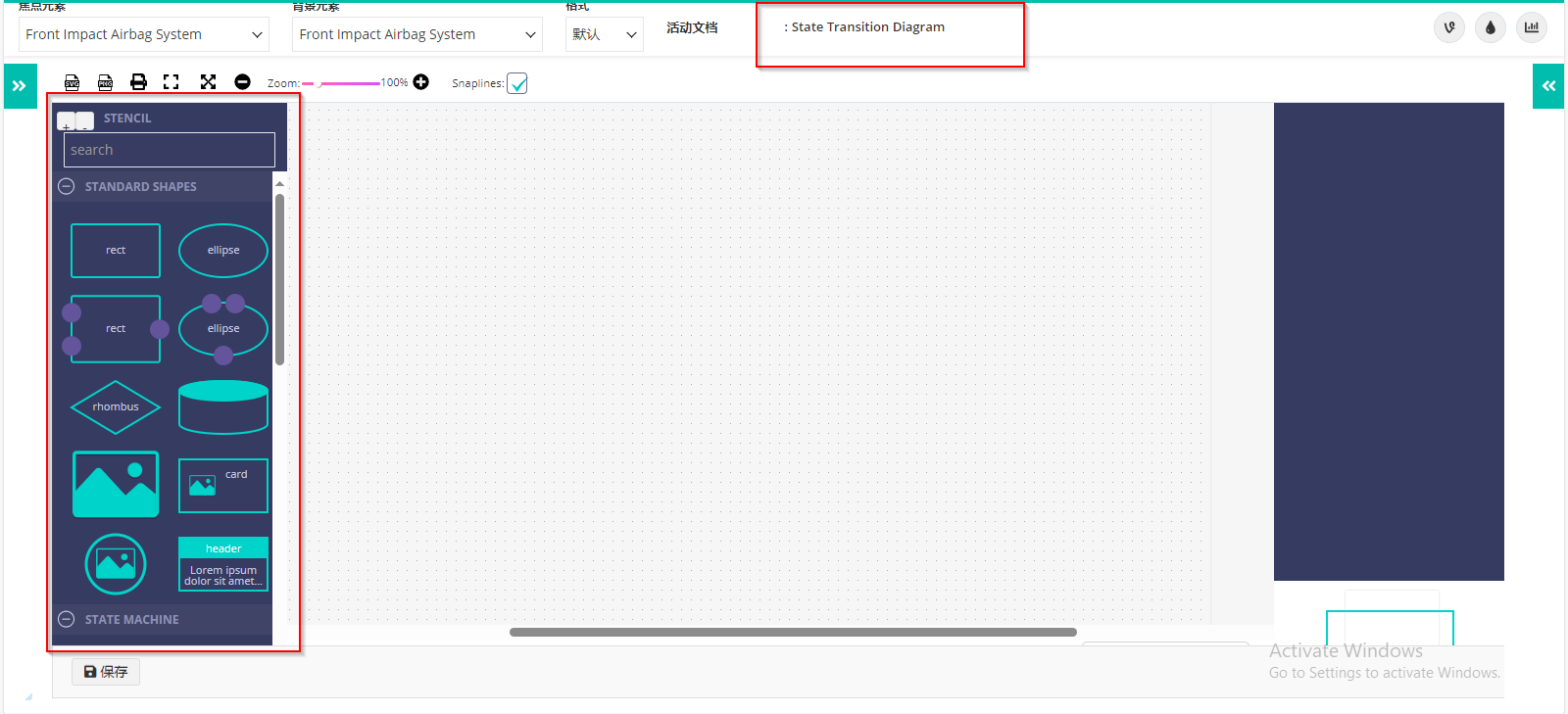
****

**P Diagram**

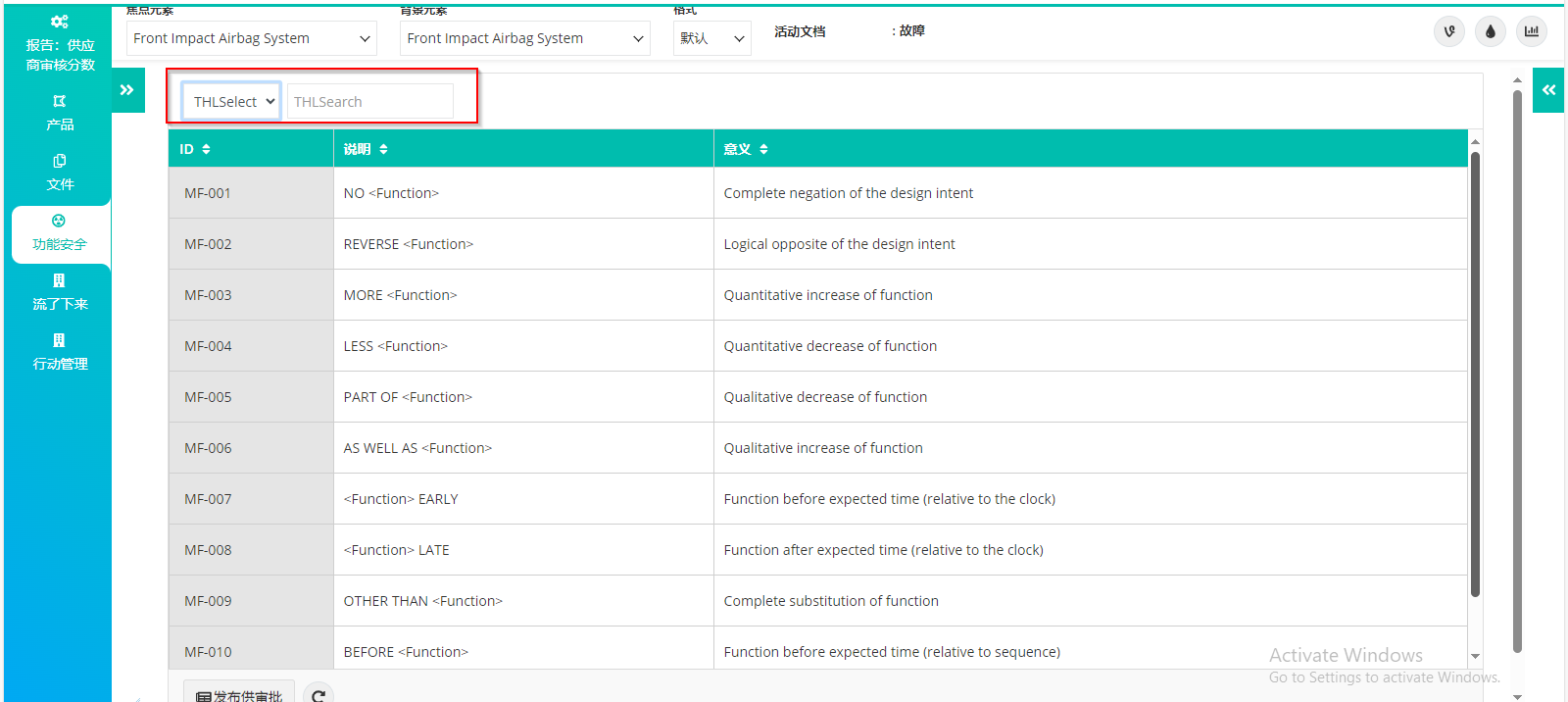
****

****

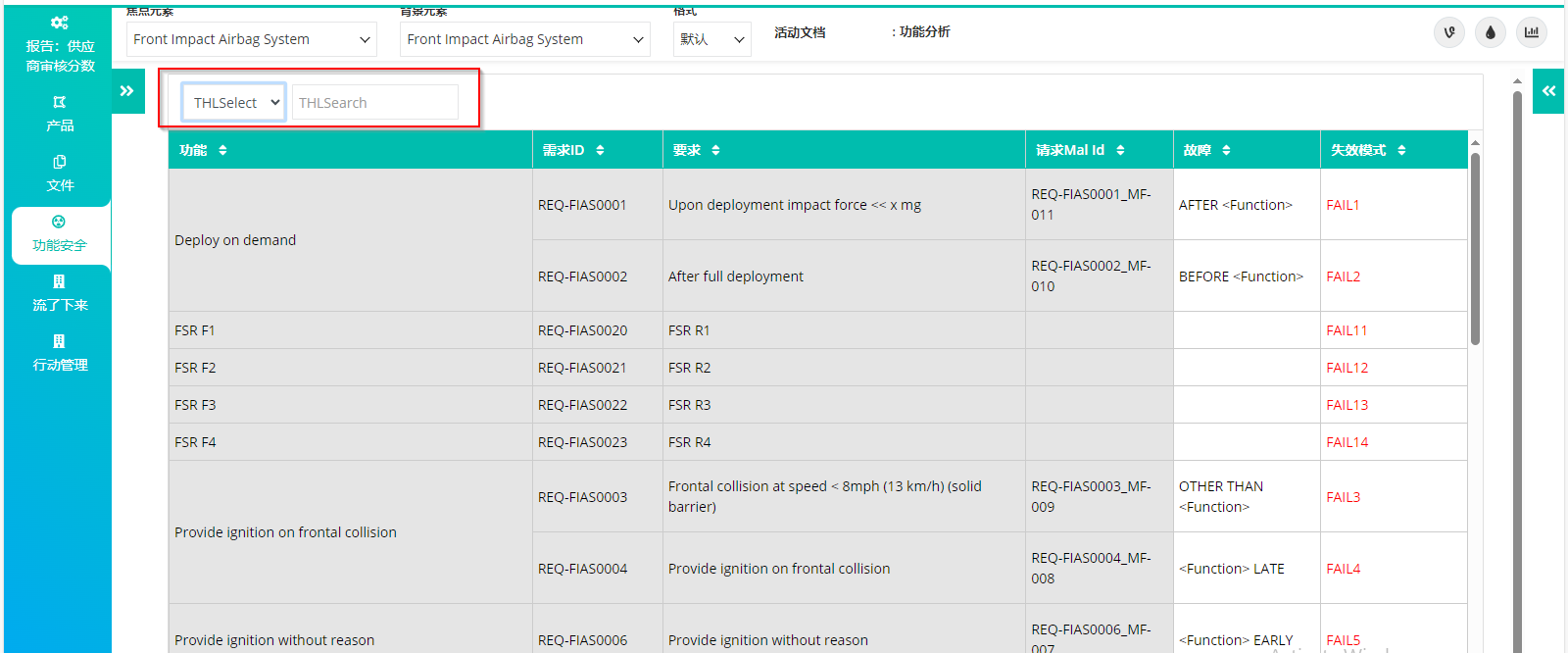
**State Transition Diagram**

****

**Malfunction**

****

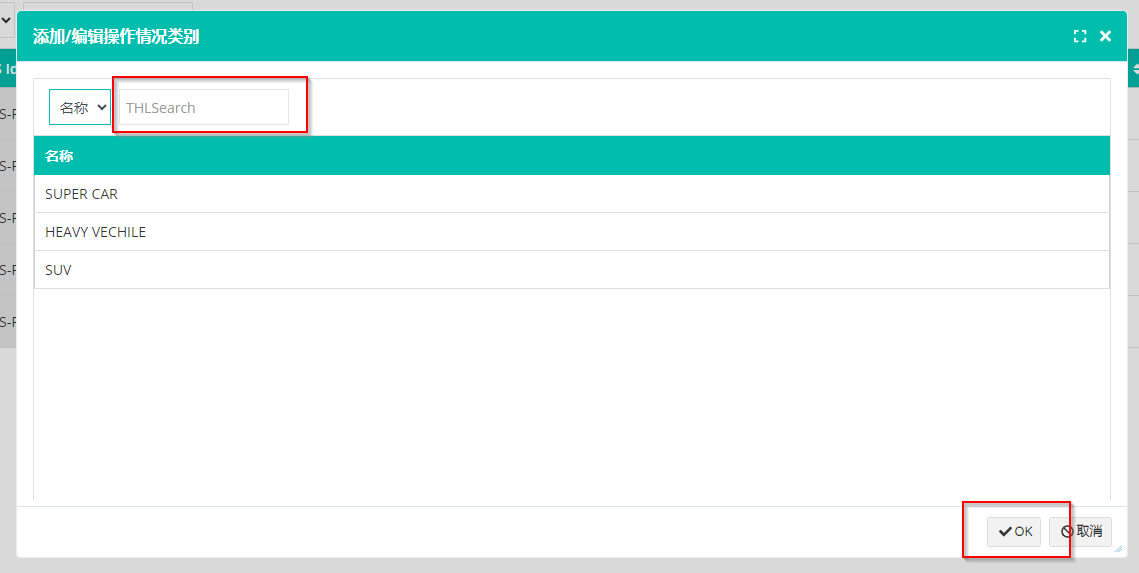
**Functional Analysis**

****

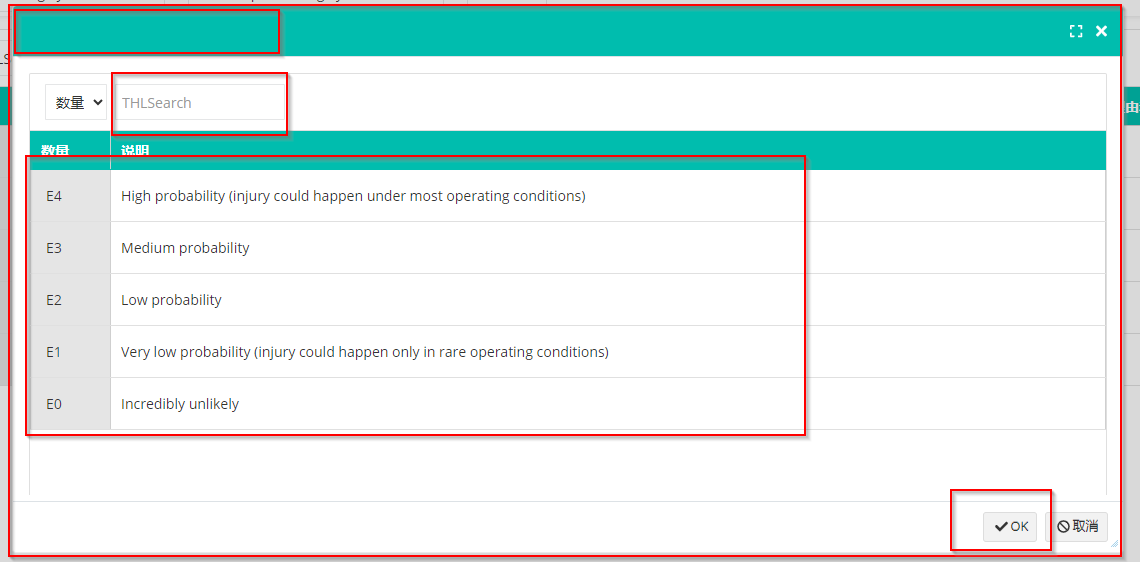
**Operational Situation**

****

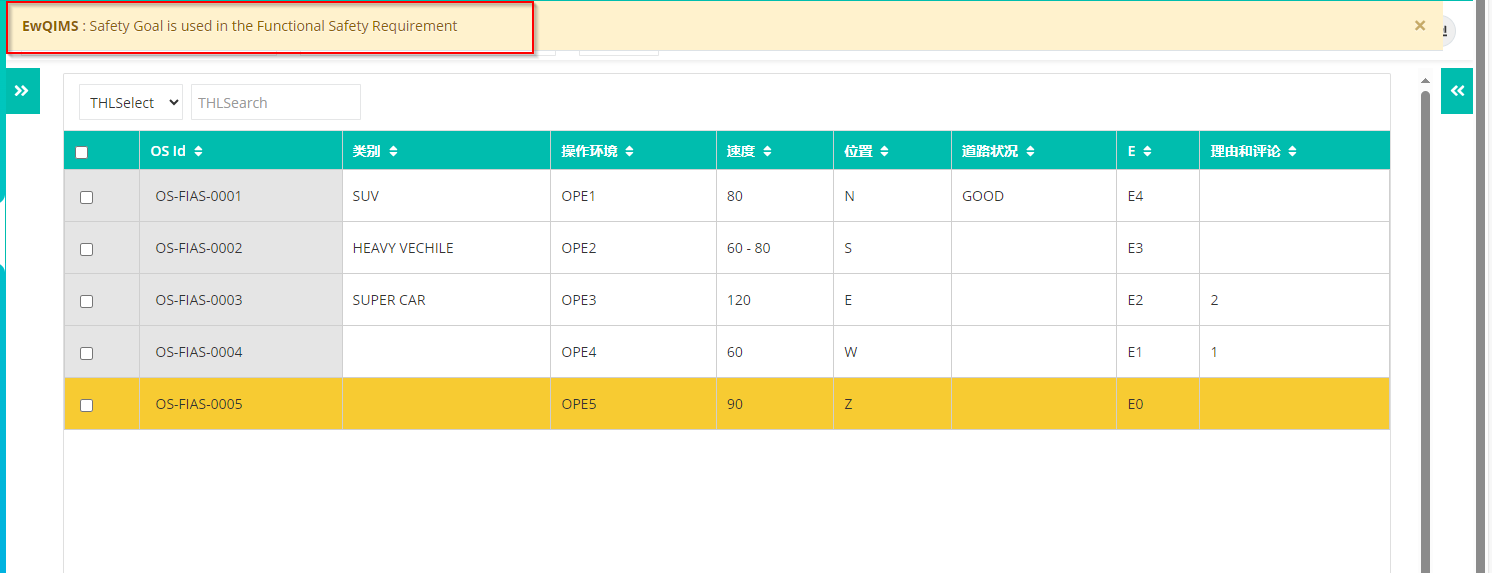
**Category**

****

**Exposure**



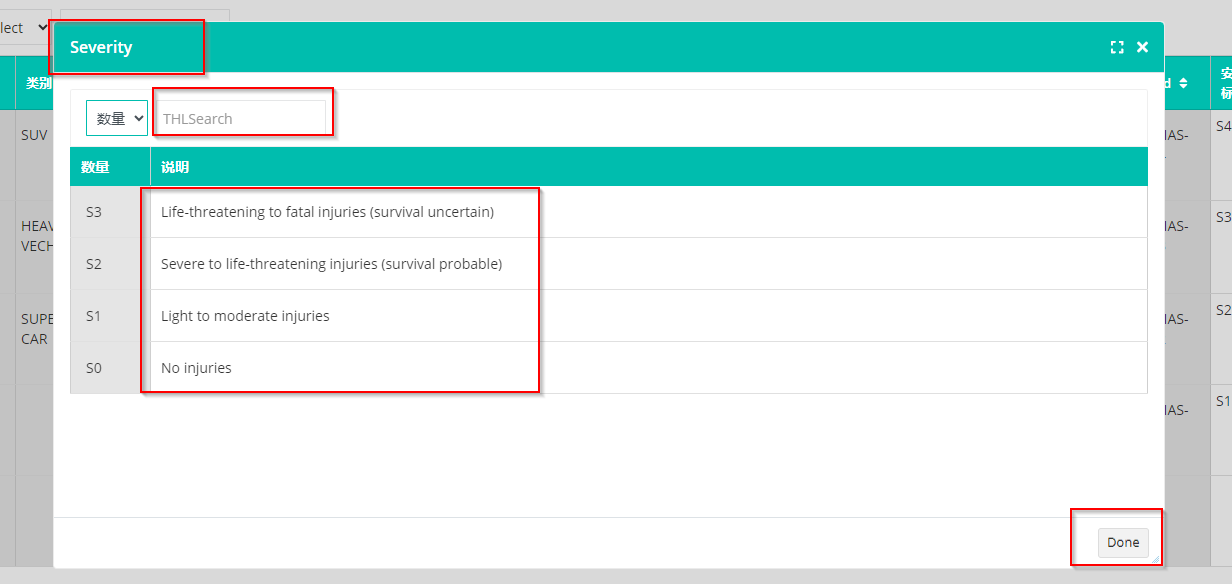
**Alert**

****

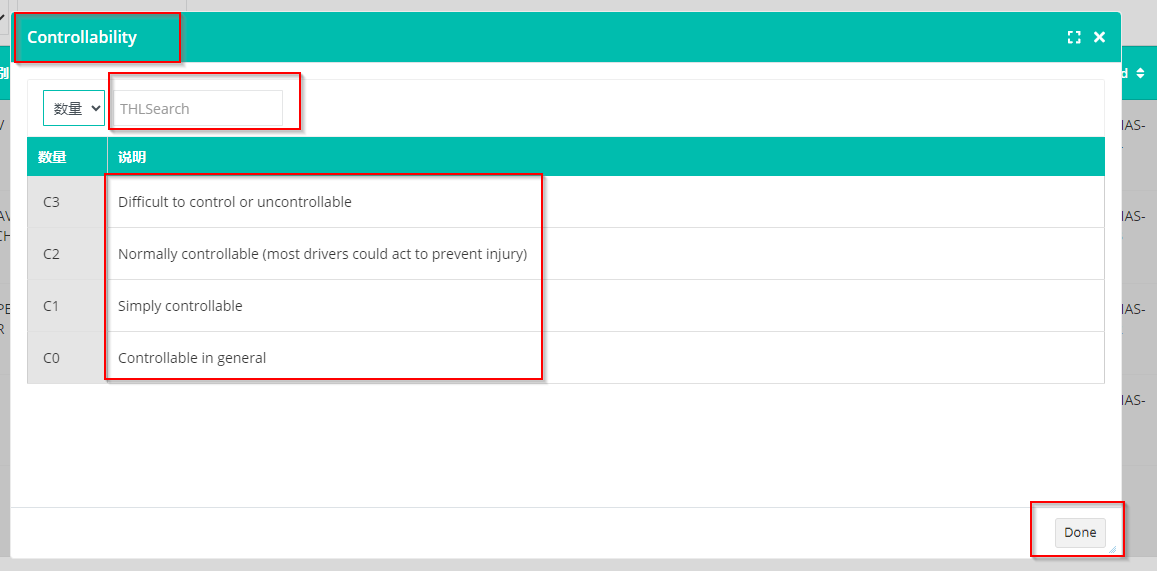
**HARA**

****

**Severity**

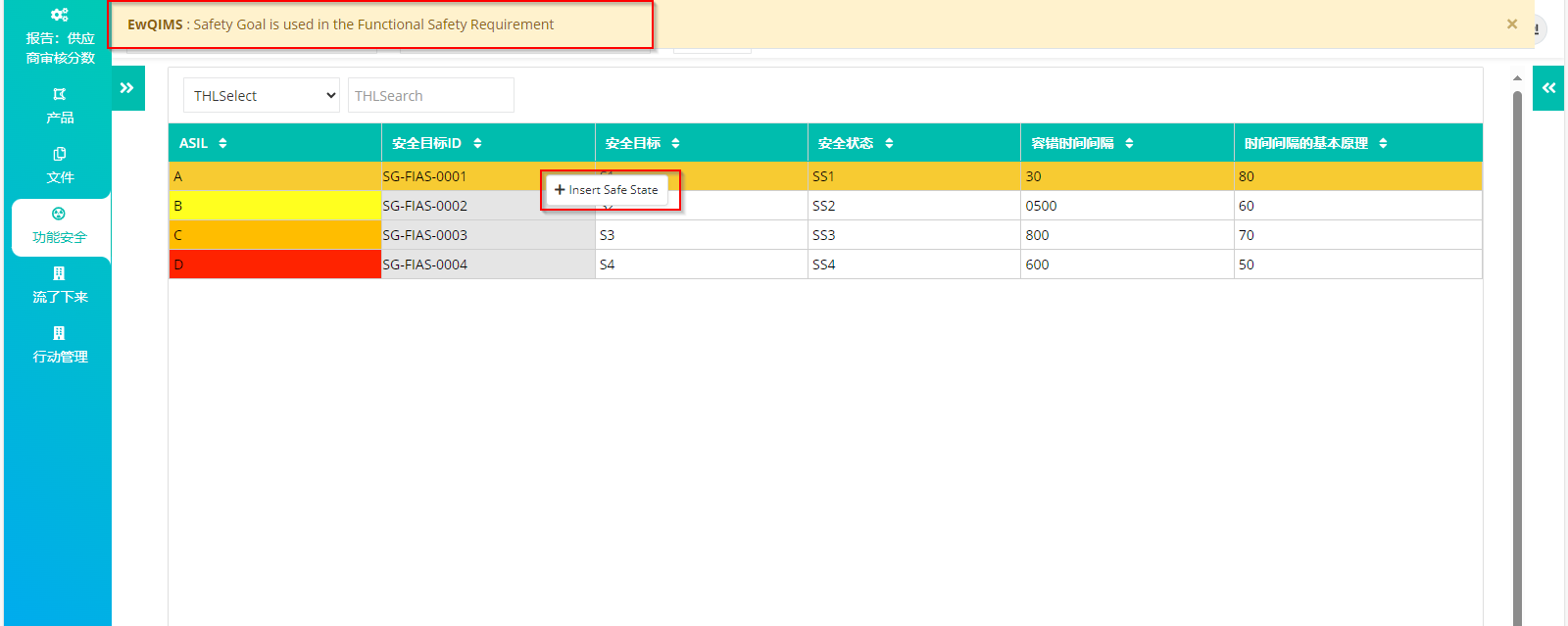
****

**Controllability**

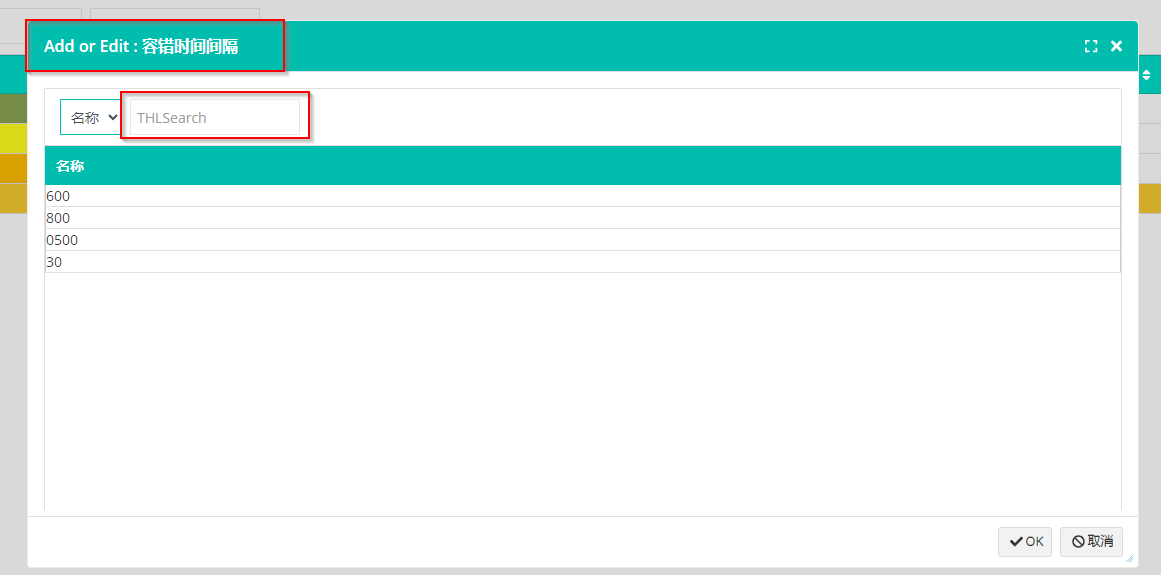
****

**Safety Goal**

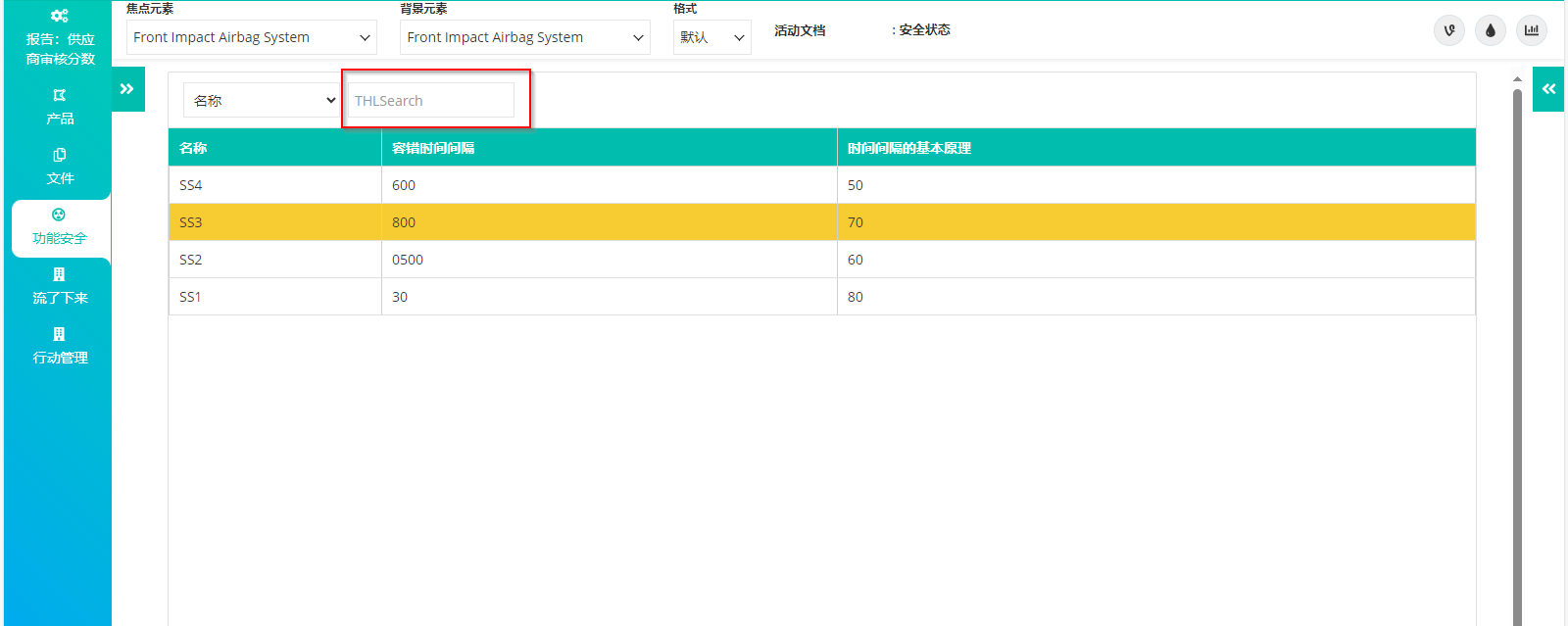
****

****

**Fault Tolerant Time Interval & Rationale for Time Interval**

****

**Safe state**

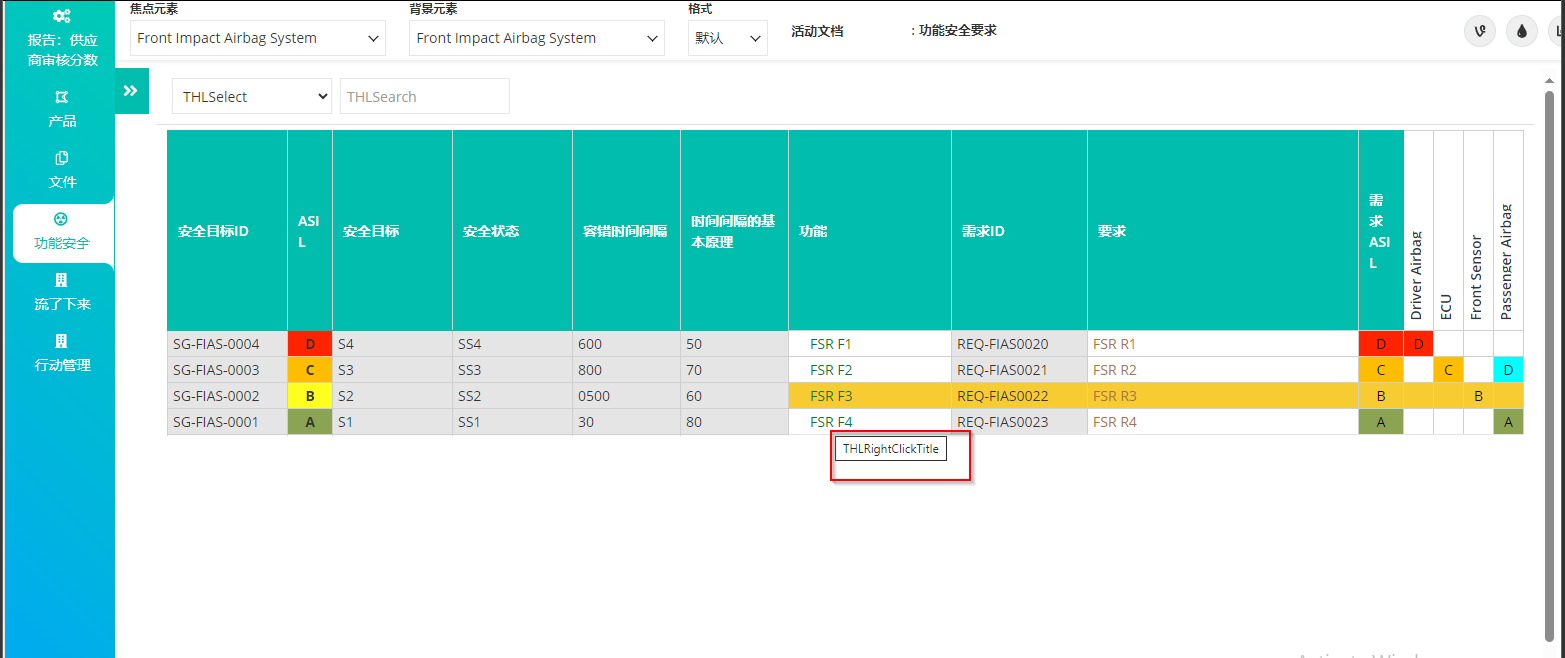
****

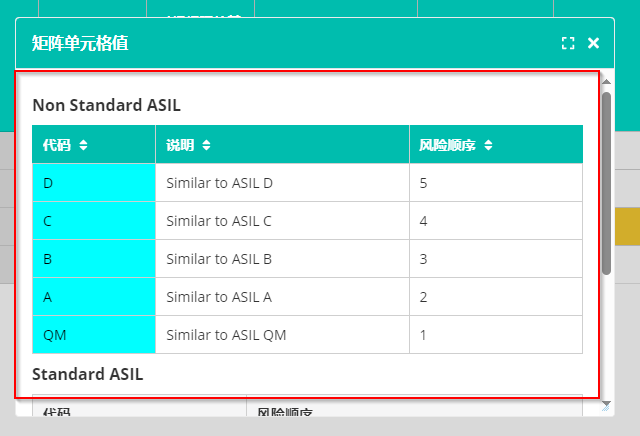
**FSR**

****

**Non-Standard ASIL**

****

****

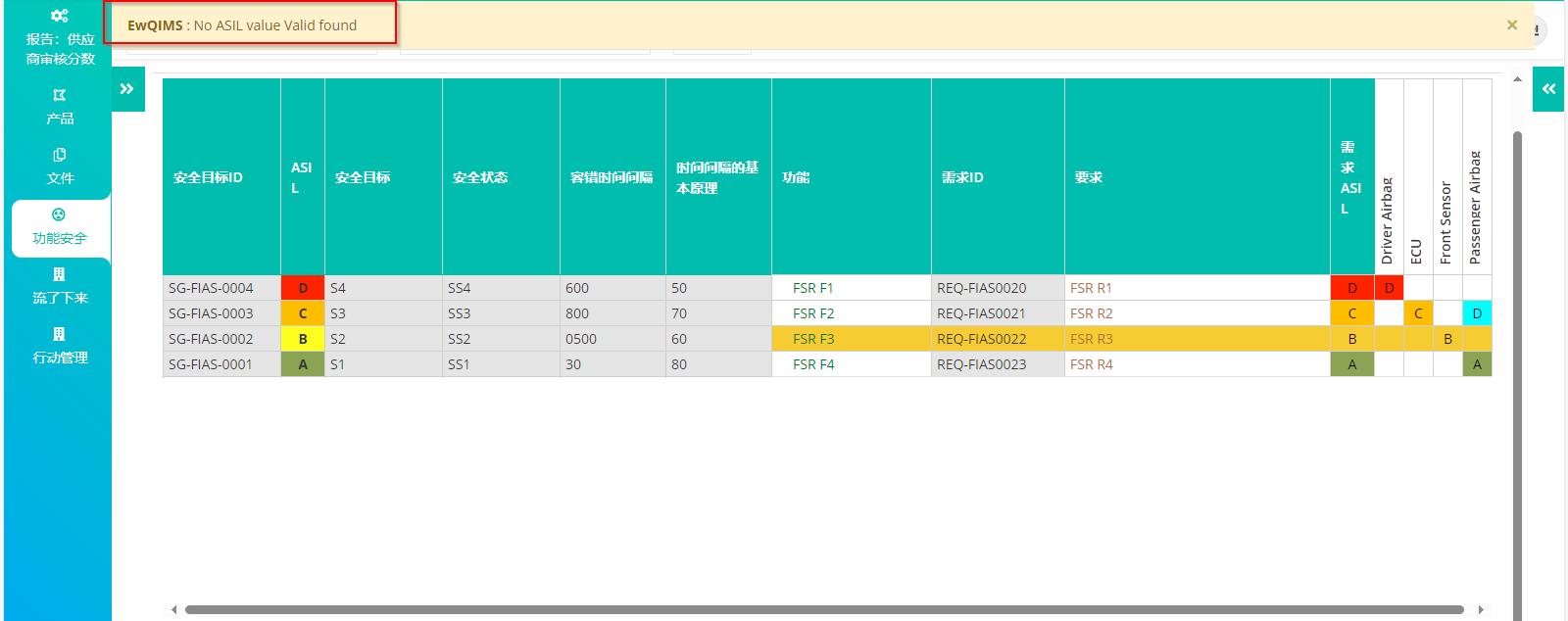
****

**Add From DFMEA**

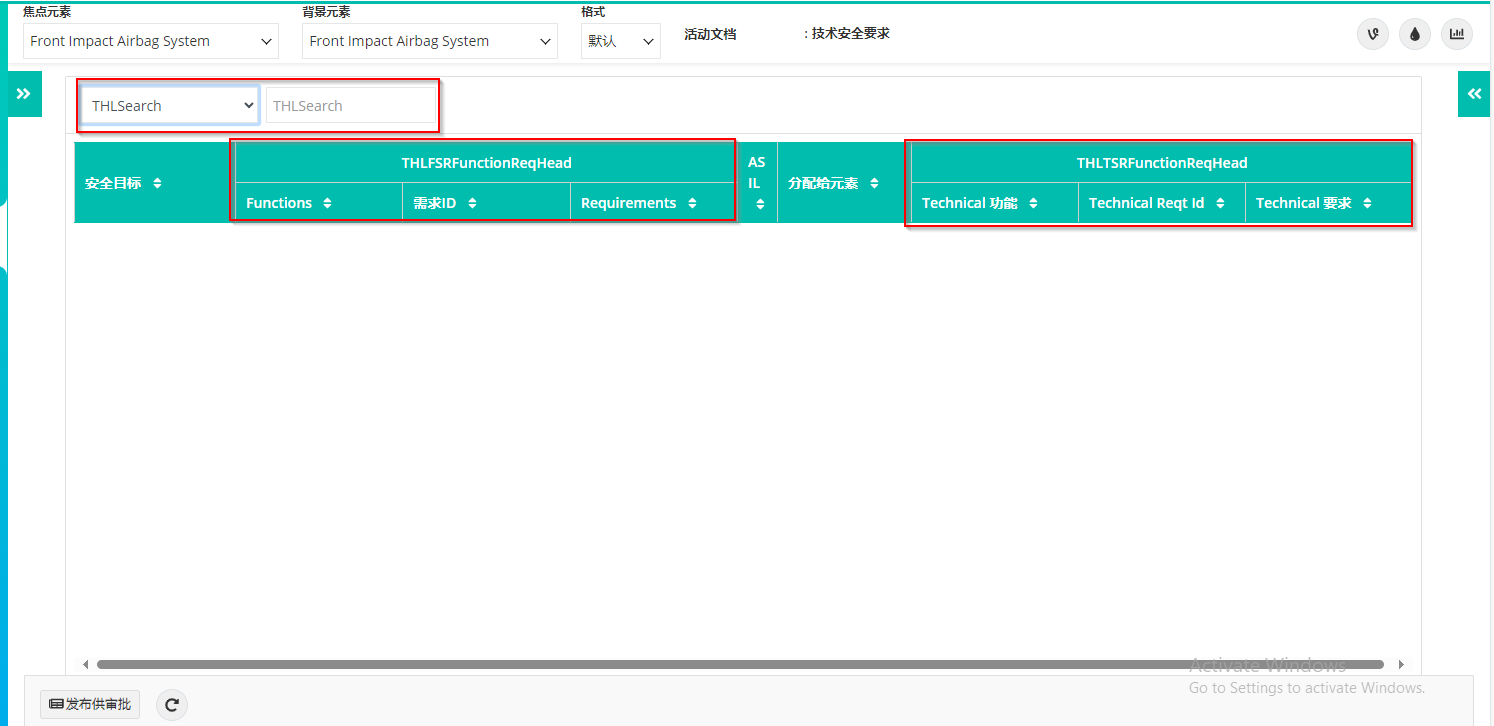
****

**Show and Hide Allocation is not working**

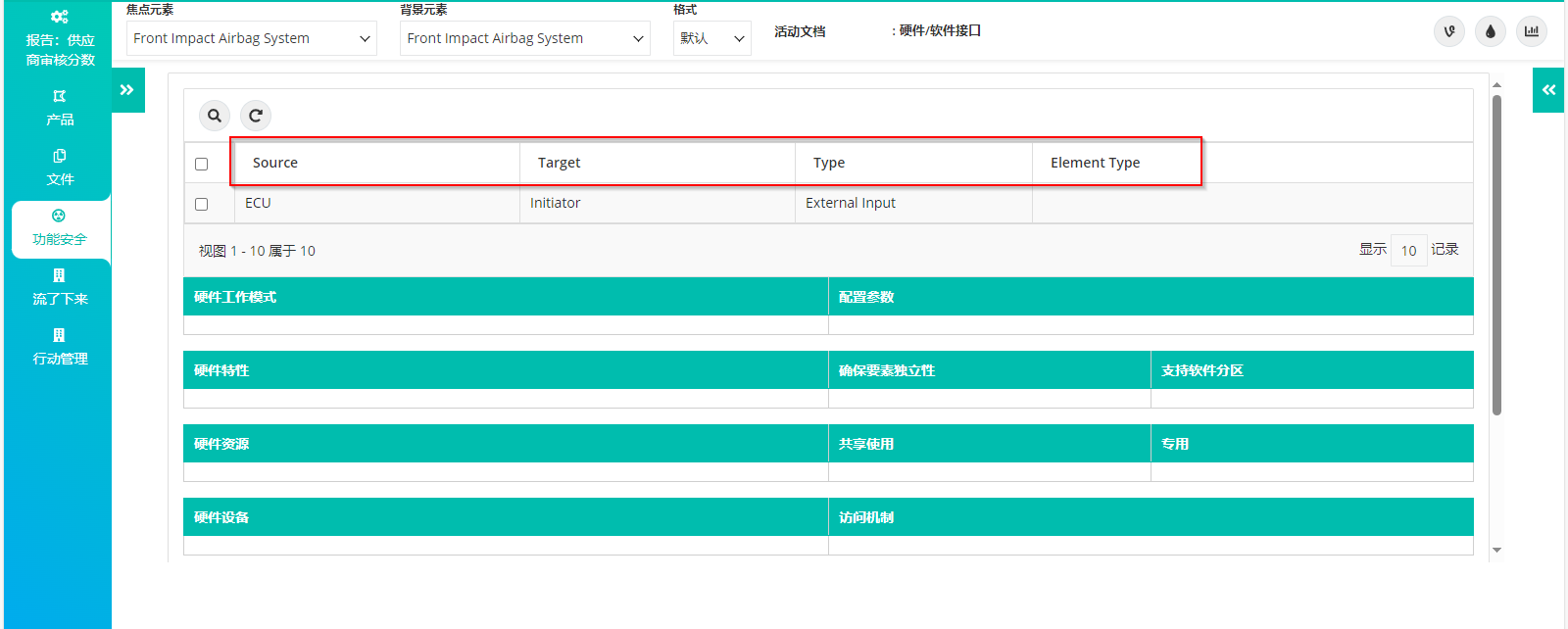
****

****

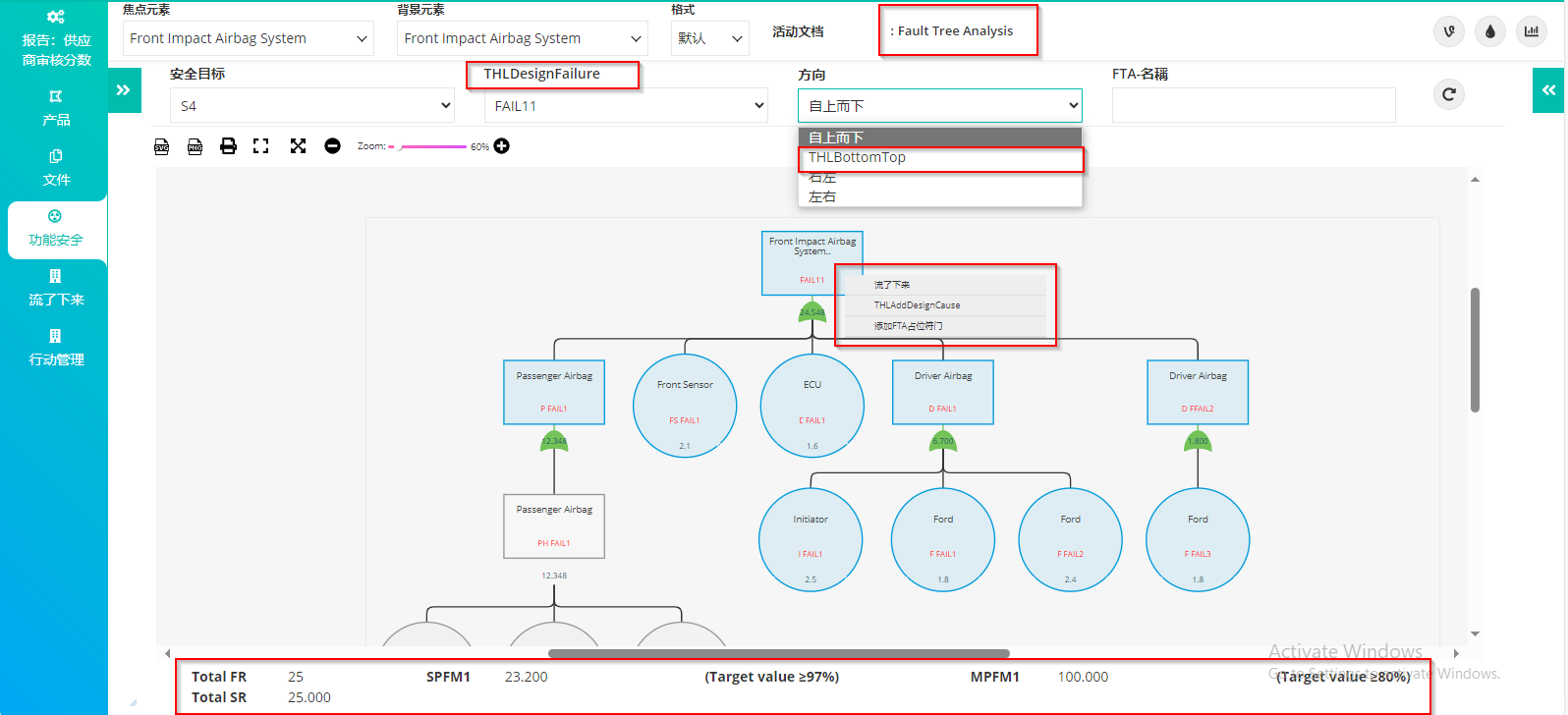
**TSR**

****

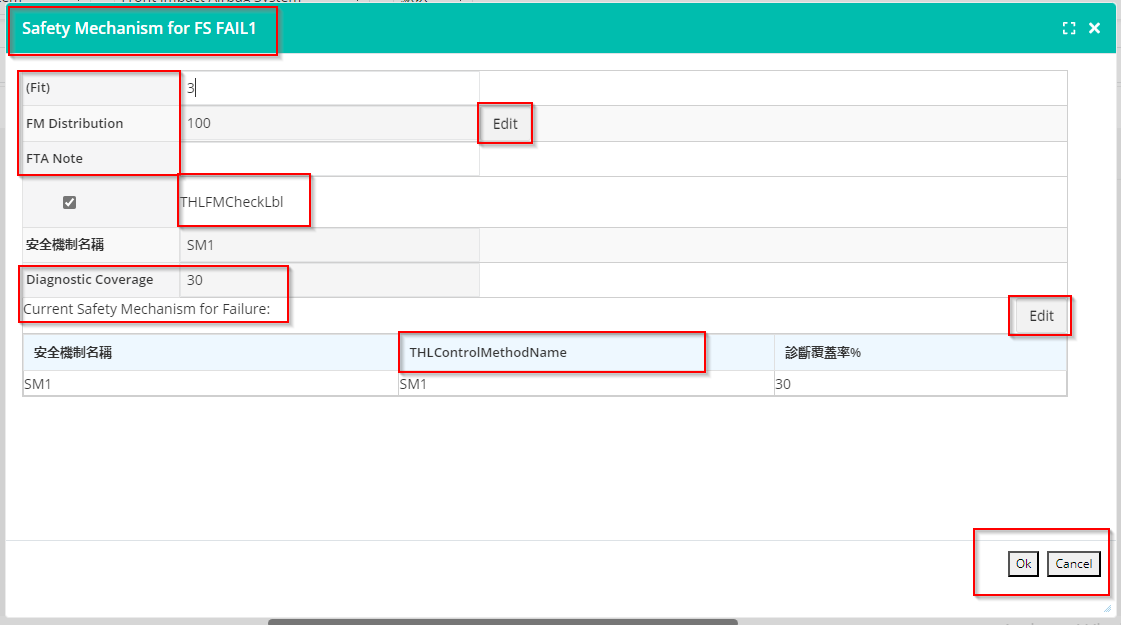
**Hardware/Software Interface**

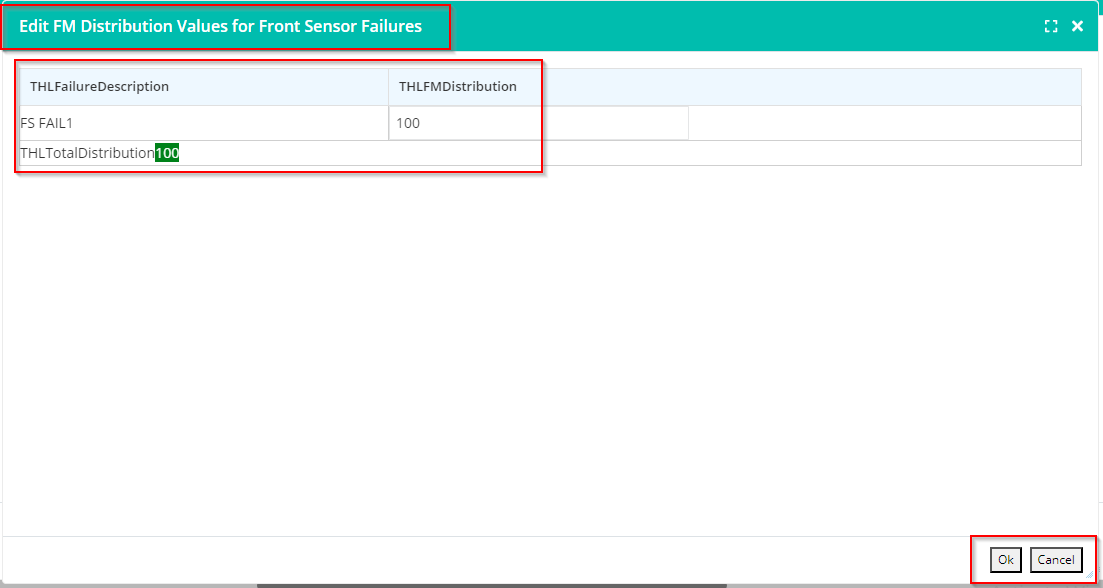
****

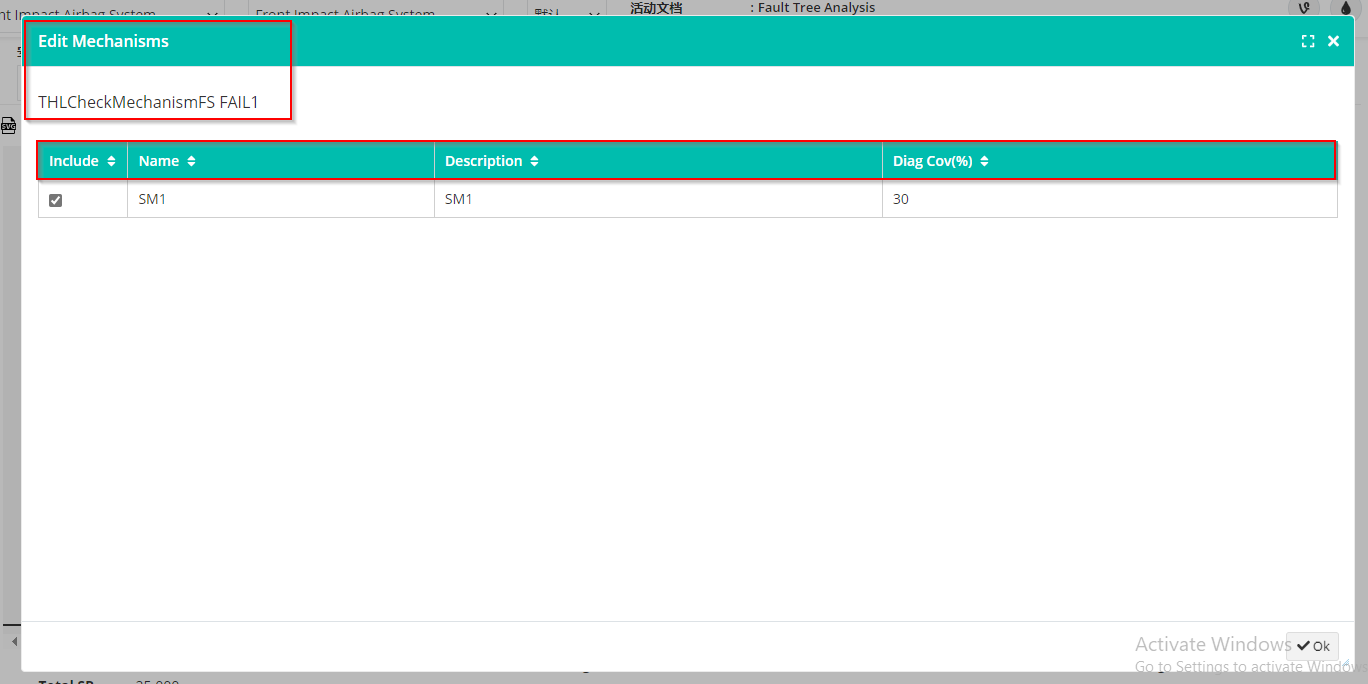
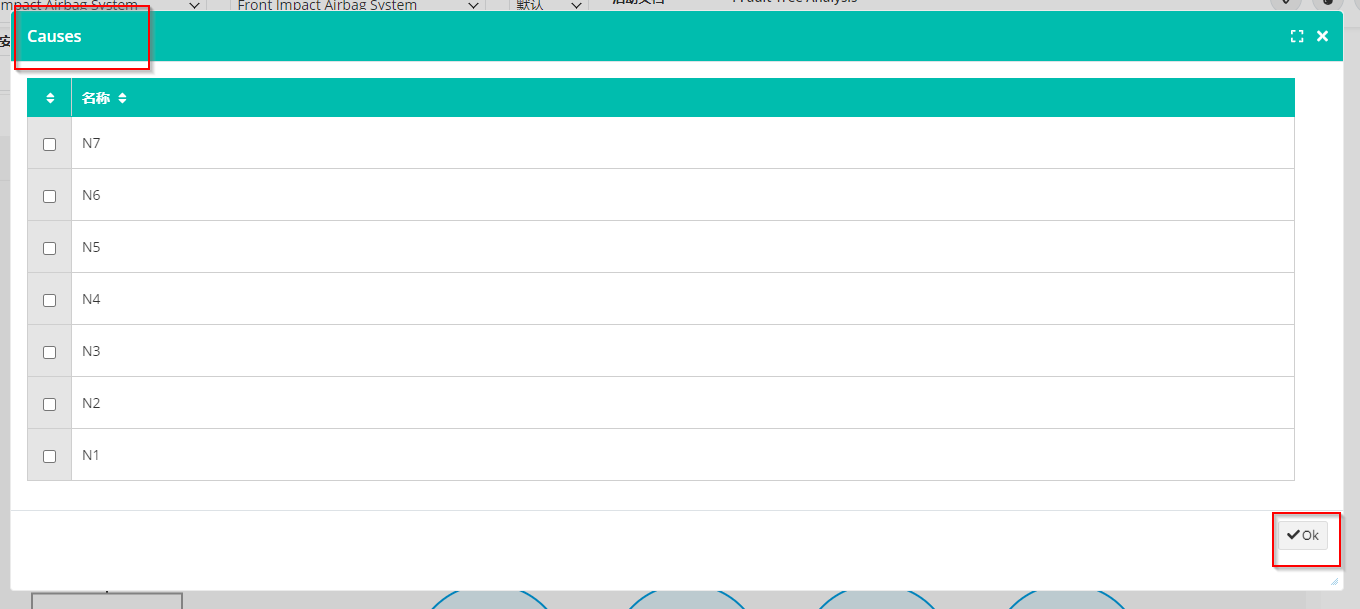
**FTA**

****

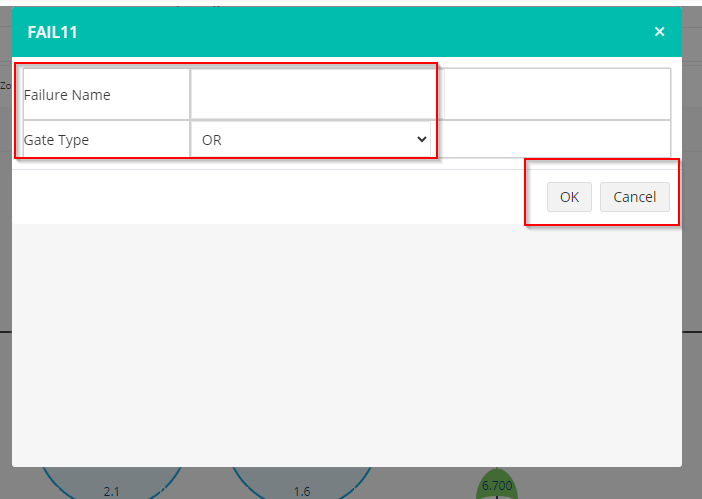
**Add Probability**

****

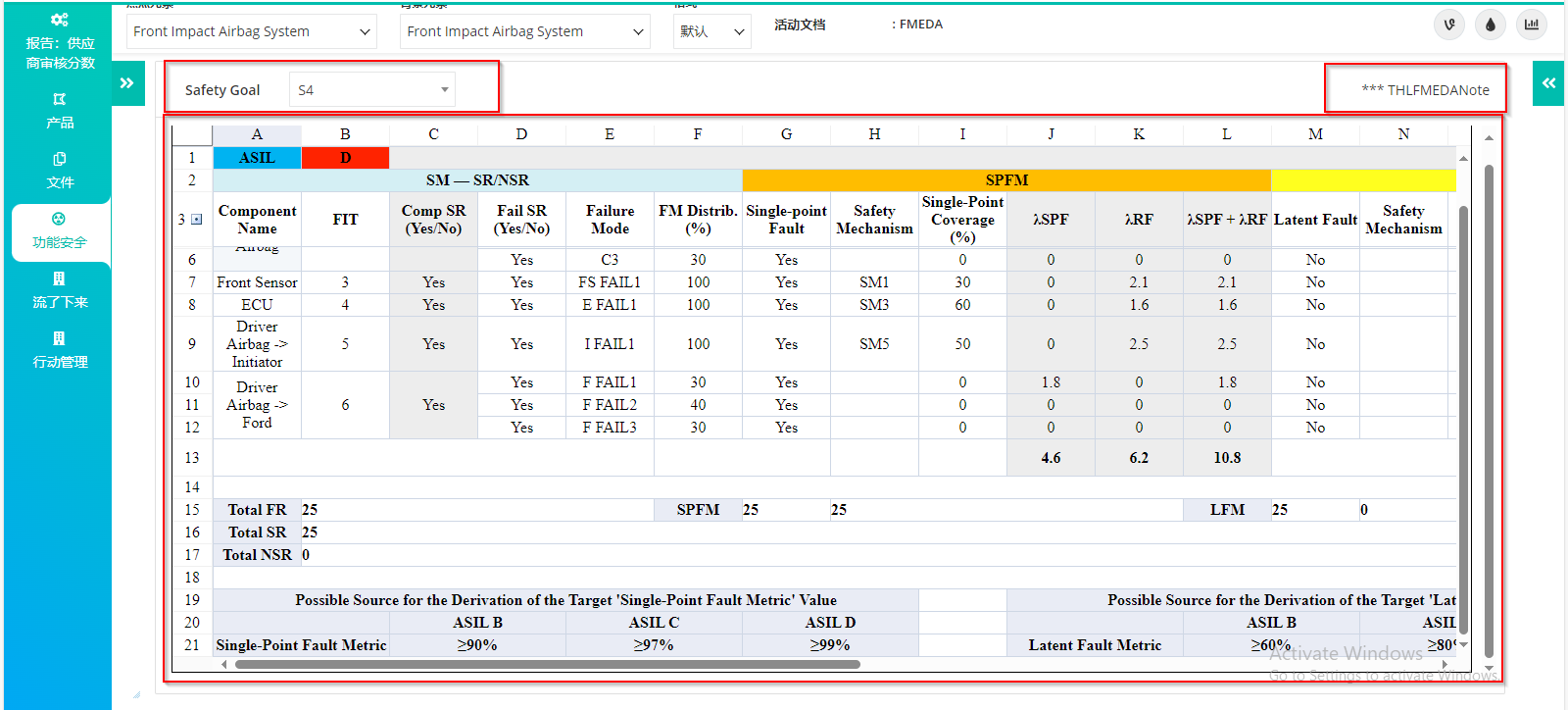
****

**Cause**

**Placeholder**

****

**FMEDA**

****