# 6/26 Issue 13 – FTA Creating Too Many Gate Type ATIs Created

Reported 06/26/2021

* After changing an OR Gate to an AND Gate:

 

* FTA is creating DFailU.FTA Gate Types for every PI and for both DFailUs under the gate:

 

* This is incorrect in two ways. The Gate Type should be set only for the DFailU using DFail *1.2 does not meet radiation* (1) and only in context of Element BMS Software (2), since the AND gate is representing this DFailU/DFail and not the two below it.
* This is indicated in the picture **FMEDA and FTA Documents\Common\MSS Engine Example\MSS Engine-120-FTA-Engine, DFail1-Page 035-Final Model.png** sent as part of the 10.0.0 patch containing the AQuAPro implementation of the FMEDA and FTA. The following picture has been rearranged to show the same information:

